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SPIRE WE Group meeting #3 - Saclay - July 19-20, 1999

Attendees: IFSI : R.Cerulli, R.Orfei
RAL : K.King
SO : H.G.Floren, G.Olofson
LAS : D.Ferrand (second day)
SAp : L.Rodriguez, C.Cara, F.Loubère

1. Action review.

1.1 Action from WEG meetings

- **WEG meeting #2 - Saclay - May 6, 1999**

Action 1	JLA	asap	Closed	Circulate the preliminary draft of the WE Requirement Document.

- **WEG meeting #1 - Saclay - March 24-25, 1999**

Action 1	KK		Open	to issue a note stating both objectives and expected inputs for the Sept. 99 PDR.

Still open. See the PDR preparation section.

Action 5	System team		Open	to perform a risk analysis.

Action 6	KK		Closed	to boost the SPIRE QA activity.

KK and JLA have met G.Douglas. Actions will be carried out by GD to form up the SPIRE QA team and set up the SPIRE QA policy by September 1999.

Action 7	RAL/GD	asap	Open	Issue the SPIRE Quality Requirements

See above.

Action 9	SAp/FL	04/99	Open	Produce the first issue of the Warm Electronics Product Assurance Plan

Started but waiting for SPIRE QA instructions.

Action 10	SAp/FL	05/99	Open	Produce the first issue of the Warm Electronics Quality requirements.

Started but waiting for SPIRE QA instructions.

Action 12	WE Inst.	06/99	Open	to produce their Product Assurance Plans.

No progress except for SAp (see above).

Action 14	System Team	01/10/99	Open	to produce redundancy requirements at system level.

Has to be written for the next System Team Meeting (Oct. 1, 1999).

1.2 Action from other meetings

- **Warm electronics & S/W working group splinter meeting (SPIRE Consortium Meeting - RAL - Dec. 1-2, 1998)**

Action 2	BMS	20/01/99	Closed	To respond the essential input request list.

Bruce responded in a mail dated May 11, 1999. Most of the info are now superseded by outcomes of meeting or various notes. Some points are still widely open like the definition and operation of the Instrument modes including the degraded modes (this includes FTS operation and readout synchronisation).

Action 3	KJK	15/12/99	Closed	To provide a Development Plan containing AIV information as well..

A new version of the SPIRE Instrument Development Plan has been issued (draft 0.2, June 23, 1999). It contains general AIV info but the SPIRE overall schedule is still missing as well as the delivery milestones (delivery of the various WE models by SAp to RAL). By the way, the exact content of each delivery (product, documentation) should be stated somewhere.

- **SAp/IFSI meeting - IFSI - Feb. 16, 1999**

Action 2	IFSI & SAp	15/03/99	Superse ded	Comment the preliminary draft of the SPIRE Development Plan.

- **CWG #4 - Feb. 10, 1999**

Action 3	JLA	20/05/99	Superse ded	SPIRE to confirm allocation of responsibilities for SPU h/w & s/w implementation.

No more SPU.

Action 5	IRC (*)	06/05/99	Superse ded	Generate and Co-ordinate "requirements" on instrument commanding & verification.

Action 7	RC/JLA	06/05/99	Superse ded	Define OBSW related milestones and activities till end 99.

Action 8	KK	06/05/99	Superseded	Provide comments to Appendix 1 of Mission Operation Scenario.

- **CWG #3 - Feb. 3, 1999**

Action 3	KK	19/05/99	Closed	Provide plans for ILTs, indicating required deliveries (S/C simulator, CCE,...)

Part of the Development Plan.

Action 8	KK	30/04/99	Closed	Comment on PACS RTA requirements used for SCOS testing.

Action 9	KK	05/03/99	Closed	To supply estimates of manpower available for RTA related activities.

- **CWG #1 #2 - March 3, 1999**

Action 1	RO	25/05/99	Closed	Submit list of needed common parts.

IFSI provided a component list. Update is foreseen by September 1999 (see below).

- **CWG #1 #2 - July 2, 1999**

Action 2	All teams	01/11/99	Open	to define any need of special timing signals, in particular their accuracy, from the OBDH.

The OBDH provide 20ms timing accuracy. To be checked at the System level (is it compatible with all modes?).

Action 1	All teams	15/09/99	Open	to update their part list.

2. Outcomes of PDR 1 and possible impact on WE.

a. A lot of open points are remaining. Among else:
   . the operation of the instrument.
   . the instrument design itself and especially the FTS.
b. KK: we have to work on assumptions. When several possibilities can be considered, impact on electronics, system or science has to be evaluated.
c. JLA: one of the recommendation of the board is that SPIRE has to perform simulations. Result of simulations could have impact on the WE.
d. CC: The production of simulated scientific data is needed for both s/w and h/w design.
e. OG: Compression issues. Glitches have to be taken into consideration.
f. Degraded modes: SAp stated that the WE cannot be designed to compensate the consequences of degraded situations. Degradation of the performances have to be considered and accepted.
g. Still open FTS options could have dramatic impact on the data rate and data reduction. Outcomes are expected from the early Sept. FTS meeting. In the mean time, simulation have to be carried out.

Action 1	CC	by the next FTS meeting	Open	To analyse the possibility to implement lossless compression algorithm on both FTS and Photometer based on DC substraction.

3. WE Requirements

a. A WE requirement document has been issued (Draft 0.1, May 11, 1999). This document will be revised in particular in the light of the new version of the SPIRE IRD and the OIRD.

Action 2	JLA	09/99	Open	To Issue a revised version of the WE Requirement Document.

b. The production of the WE documentation has been briefly discussed. Discussion lead to the conclusion that a WE documentation tree has to be produced.

Action 3	FL/JLA	09/99	Open	To propose a WE documentation tree.

4. WE architecture and internal I/F

a. Presentation by CC of the new overall architecture scheme (without SPU) and of the electrical configuration.
b. Question about low rate sampling of the H/K: one per second could prove to be not enough especially in diagnostic modes. Current requirements in the SPIRE IRD is up to 1ms rate for a limited selection of H/K for diagnostic purpose. KK pointed out that there is a requirement on the OIRD giving minimum acquisition rates for diagnostic purpose as well. CC stated that these requirements will be considered as far as they are realistic.

4.1 DPU/DRCU I/F

a. The DPU/DRCU communication link interface has been discussed. This interface mainly consists in:
   . a bi-directional low rate transmission line dedicated to telecommand (+ memory load or dump). This line is based on a standard UART, with a maximum bit rate less or equal to 115 kbps and implemented with two wires (TX and RX) with RS 422 line drivers and receivers.
   Telecommand are low level and to be executed as soon as possible. Systematic acknowledge or on request to be envisaged.
   . a mono-directional (DRCU to DPU) High rate transmission line (up to 2 Mbps) used to transfer both science (detector readout) and h/k. H/K packets will be interleaved with the scientific packets. H/K packets will be time-tagged. Packet type shall be identifiable by the DPU (addition of header and trailer required).
b. Concerning the redundancy issues:
   . Cold redundancy of both DPU and the DRCU processing unit.
   . Redundancy on transmission lines have to be considered. JLA stressed that crossing lines between DPUs (Main an redundant) and the DRCU processing unit (Main and Redundant) could lead to more reliability (4 DPU/DRCU combinations instead of 2).
   . RO stressed that the DPU redundancy philosophy, i.e. one active and one in cold redundancy, is simple and the most efficient.

4.2 Power supply distribution and monitoring.

a. Discussion on Power Supply requirements (cf. "Autonomous decision modes" note from LV - Issue 1 - June 22, 1999). Requirements have to be agreed and stated. In particular, implementation of VETO systems has to be decided.
b. IFSI stated that only a low power control line (to be used to switch on/off the DRCU power supply (28V) could be envisaged. In this case the switching power is to be derived from DRCU +28V. This is however not compatible with any VETO implementation requirement.
c. IFSI stated that there is no need for the DPU to monitor the DRCU analogue signals, as these, when DRCU is ON, will be monitored by the DRCU itself, digitised and passed to the DPU. The DPU can then take agreed autonomous actions in case some of these parameters are not as expected. When DRCU is OFF, the only useful parameters are DRCU box temperature and +28V line: both parameters monitored by the S/C.

Action 4	CC	09/99	Open	Issue a recommendation for Power supply monitoring. Propose requirements

4.3 FPU subsystems I/F.

a. DRCU Internal Interfaces (see viewgraphs).
Daisy chain access. All data have to be read in one go by the DRCU and then sorted and rearranged to ground sending.
b. Synchronisation of the BSM and the detector readout controlled by the DRCU s/w.

4.4 Grounding scheme.

Not addressed.

5. DPU Development (IFSI)

a. No EM Model as such (except for IFSI development purpose).
b. The DPU is made of 4 boards + the DPU box:
- the DSP board with piggy back memory.
- the OBDH communication board.
- the DRCU communication board (likely in house design).
due to the fact that the 3 instruments will not require exactly the same interfaces, it is foreseen that this board could support all necessary components needed for the 3 instruments. For a given instrument, only the needed components will be mounted.
c. Qualification will be performed on only one (out of three) configuration.
d. Analog parameter monitoring by the DPU: could prove to be necessary due among else on decisions to be made at the next (Oct. 1, 1999) System meeting for what concerns the WE Power supply monitoring.
e. DPU Development plan:
. an overall schedule has been presented by IFSI.
. JLA stressed that the integration phase should be carefully detailed to prevent from any underestimation taking into account the involvement of IFSI in the development of the DPU for two other instruments.
f. Discussion on DPU/DRCU synchronisation: 20 ms from the OBDH could be enough for what concern the absolute time. Accurate relative timing could be achieved by the mean of local (DPU & DRCU) clocks.

Action 5	CC/LR	30/09/99	Open	Define relative timing accuracy needs.

g. IFSI stated that the ITT for the procurement of the DSP CPU boards has to be sent next week. This is mainly due to HIFI development constraint and the 1.5 year manufacturing delay.

h. JLA pointed out that, given the importance of the DPU in the WE architecture and for the instrument in general, the DPU manufacturing requirement should be at least circulated for comments before it is sent to the potential submitters (the ITT procedure allowing no significant change of the requirements). RO stressed that during the necessary delay allowed for discussion with the submitters, changes should be possible.
i. JLA stressed that, given the open points raised during this meeting, the requirement sent to the submitters have to leave flexibility in the following areas:
   - Power supply monitoring.
   - Harness redundancy between DPU and DRCU.
   - Analog parameter monitoring by the DPU (for power supply monitoring purpose).
j. JLA stressed that special care should be taken for what concern the board performances: these performances have to be considered not only on the H/W point of view but on both h/w and s/w point of view.
   As an example, the communication link performances could be met (theoretically) but if it burden the s/w too heavily (e.g. handling of huge interrupt rate) the actual performance (h/w + s/w) could prove to be inadequate.
k. IFSI stressed that given that the ITT has be be sent only to Italian companies (ASI requirement), the DPU specifications have been written in Italian. However an old version written in English is existing and will be circulated for comment.
l. Link performance in burst mode: it has been suggested that the minimum requirement could be based on the real time sending of a whole interferogram.

Action 6	IFSI	21/07/99	Open	Send out the specification of the DPU board.

Action 7	WE Team + System team	30/07/99	Open	Send comments on the specification of the DPU board to SAp (JLA)

Action 8	SAp	02/08/99	Open	Send the compiled comments on the specification of the DPU board to IFSI

Action 9	IFSI	06/08/99	Open	IFSI to reply on the comments on the specification of the DPU board and take the appropriate actions if necessary.

6. S/W development:

a. WE S/W requirement document has to be written first. DPU/DRCU sharing will then lead to the writing of separate s/w requirement document for the DPU and for the DRCU. DPU/DRCU ICD will contain the description of the s/w interface.
b. Development at IFSI:
   - IFSI have placed order for the procurement of the necessary s/w development environment for the DSP.
   - S/W development resources: 3 EM requested. 3 development stations, 3 developers + 1 development manager.
c. Development at SAp.:
   - Activity not yet started.

7. Support Equipment

7.1 Test equipments:

7.1.1 EGSE.

a. KK stressed that no decision has been taken yet about the responsibility of the development of the EGSE (awaiting reply from the Canadian).
b. Availability of the EGSE is an important issue: Test of the DPU, Integration of the WE electronics,...
c. EGSE requirements unclear.

7.1.2 Local Test unit.

a. Developed by the SAp for internal use: DRCU Test and Integration).
b. Requirements TBW.

7.1.3 Factory Support Equipment.

a. They are simple test facilities used for instance for DRCU subsystem testing.
b. Needs identified in the development plan and especially the AIV plan.

7.2 Simulators:

7.2.1 Cold FPU Simulator.

a. This simulator is intended for DRCU h/w and s/w testing and validation (during the development phase as well as in case of needed in flight modification).
b. Its specification should stem from test and validation plans.
c. It should simulate breakdown to some extent.
d. DF raised the issue of the interface for some DRCU subsystems like the FTS mechanism electronics. This interface is likely impossible to simulate due to the strong interaction between the electronics and the mechanics. This could be the case for the BSM electronics subsystem (TBC). For the FTS, DF suggested to use a h/w mock-up (test bench to be provided by LAS) of the FTS mirror moving system.

7.2.2 DRCU Simulator

a. Main purpose: DPU test (IFSI), DPU Acceptance Test and Integration (SAp), AVM sub-unit (ESA).
b. The h/w interface should likely not be a problem: standard serial link + high rate link likely to be implemented from standard PC interface board.
c. The DRCU simulator shall be able to simulate normal and odd behaviour of the instrument.
d. A user friendly operator interface should allow easy parameter display (result of received telecommand) as well as the programmation of the behaviour of the instrument (breakdown simulation)
e. Loggin capabilities (e.g. list of the received telecommand) shall be implemented as well.
f. SO stated that an extra station should likely be used to support the operator interface.
g. The requirement for the DRCU simulator should stem from:
   - the functional behaviour of the instrument.
   - the On board S/W requirement and I/F description.
   - the operation requirements.
h. the first version of the DRCU simulator should be ready for EM testing.

8. Development Plan:

8.1 Production of the WE development plan.

a. JLA stressed that both for the PDR preparation and to start an active management process the production of a WE development plan is needed at short notice.
b. JLA asked the various institutes involved in the development of electronics subsystems to participate in the elaboration of this plan by sending their contribution. A template (based on the development plan produced by SAp for the CEA's detector) has been presented (see viewgraphs).
c. JLA stressed that this plan should contain all the necessary information to get a reliable appreciation on the status of the WE electronics development. Regular (monthly TBC) report should be based on this plan.
d. KK stressed that no WE development plan is needed as it is redundant with in the SPIRE development plan.
e. JLA stressed that the SPIRE development plan clearly indicates that the WE is a SPIRE Unit leaded by a Manager. The reporting flow from the local managers to the project manager through the unit managers is clearly indicated as well.

f. Waiting for clarification, no action on the production of the WE development plan contributions has been taken.

8.2 Overall AIV plan.

a. CC presented an Overall WE AIV flow chart.
b. LR pointed out that DPU+DRCU+BAU room temperature tests are not necessarily needed.
c. KK pointed out that the harness have not been considered

8.2 Beam Steering Mirror issue.

a. SAp pointed out that they have yet no hint about the development of the BSM electronics (who is doing what).
b. KK pointed out that the BMS will be designed at Edinburg but that the SAp is in charge of the development of the BMS electronics.
c. SAp stressed that the Beam Steering system turned out to be quite complex. It should be built, tested and qualified along with its electronics and delivered to SAp as a subsystem the same way it is carried out with the FTS mirror moving system.

Action 10	KK,MG		Open	To clarify the situation regarding the BSM development responsibilities.

9. Quality Assurance.

a. Awaiting for SPIRE QA instruction (G.Douglas). KK stated that a PA group will be set up within a couple of weeks (likely Sept. 99)
b. Works on components, Works on MMS board.

10. PDR preparation:

a. The Internal review will follow the same scheme as the final PDR (March 2000).
b. JLA pointed out that, for what concern the WE, the PDR approach should be somewhat different than the PDR 1. Taking into account that there are in fact no real technical challenge (use of well known technology). It should rather be more Development approach oriented.

Action 11	KK,MG	02/08/99	Open	Propose a layout for the WE review to be commented.

11. Next WE meeting:

A WE Group meeting should take place before the Internal review (Nov. 1999). It is proposed that this meeting take place by the end of September. Possibly coupled with the Oct 1 System meeting (TBC).