Systems Team Meeting

Caltech

19 May 1999

Viewgraphs

Summary of actions			
Number	Responsible	Action	Due
1	CRC	Include all relevant people in forthcoming System Team teleconferences to address critical issues for PDR.	
2	KJK	Write note to Steering Group making formal recommendation on warm electronics architecture	May 26
3	MJG	Distruibute this note to Steering Group and set up meeting/teleconference to make decision.	June 7
4	WKG + J-PB	Provide advice on what elements of arrays need to be preserved in the event of partial faiulure (e.g. squares, strips?)	June 20
5	BMS	Decide on number of calibration sources (in consultation with MJG, J-P B, SHM, et al.)	June 20
6	CRC	Analyse and document critical cryoharness wires	June 30
7	J-LA	Consider options for redundancy in warm electronics esp. DPU-DRCU connection.	Next Systems Mtg.
8	J-LA	Update warm electronics model table in the light of possible decision on deletion of SPU.	
9	BMS, MJG, CRC	Define what level of thermal analysis is needed for the July PDR.	May 27
10	MJG	E-mail Thomas Passcogel about status of warm electronics power availability	June 1
11	BMS	Raise Mech. design drawings for IID-B at May 27 Structure meeting	May 27
12	KD	Raise alignment and stability requirements for IID-B at May 27 Structure meeting	May 27
13	MJG, BMS, CRC	Define plan for thermal model treatement at PDR by May 27th Structure meeting	May 27
14	Array groups: JJB, GV, LR	Comment on proposed CEA grounding scheme	June 15
15	Array groups: JJB, GV, LR	Provide information on frequency plan to CRC	June 15
16	KJK, MSSL, KD	Provide notes on EGSE, MGSE and OGSE for IID-B to CRC	June 15
17	GV	Provide BAU design to CRC by mid-June	June 15
18 19	All Systems Team members	Review Scientific Pointing Modes Document and provide input (requirements/questions) to MJG prior to the meeting.	June 5
20	MJG	Include discussion of how instrumetnsensitivity and simulations are to be included in PDR Phase 1 in Det. Mtg. Simulations session	May 20
21	LV	Draw up draft of autonomy requirements for IRD BMS can then transfer it into IRD form	June 20
22	CRC	Write section on EMC for IRD and send to BMS	June 20
23	KJK	Provide input on redundancy to BMS	June 20
24	CRC	Provide input on FPU internal harness and budgets requirements to BMS	June 20
25	KJK	Write draft of Instrument Operations section in consultation with MJG, project scientists etc.	June 20
	MJG, CRC, BMS, KJK	Review draft IRD	June 27

25	MJG	Write to Co-Is emphasising the need for Institute Project Managers to provide KJK with essential information and to regard deadlines seriously	May 26
26	All Institute PMS	Draw up table of deliverables for subsystems and models	June 11
27	All Institute PMS	Provide Subsystem Development Plans	June 11

Agenda:

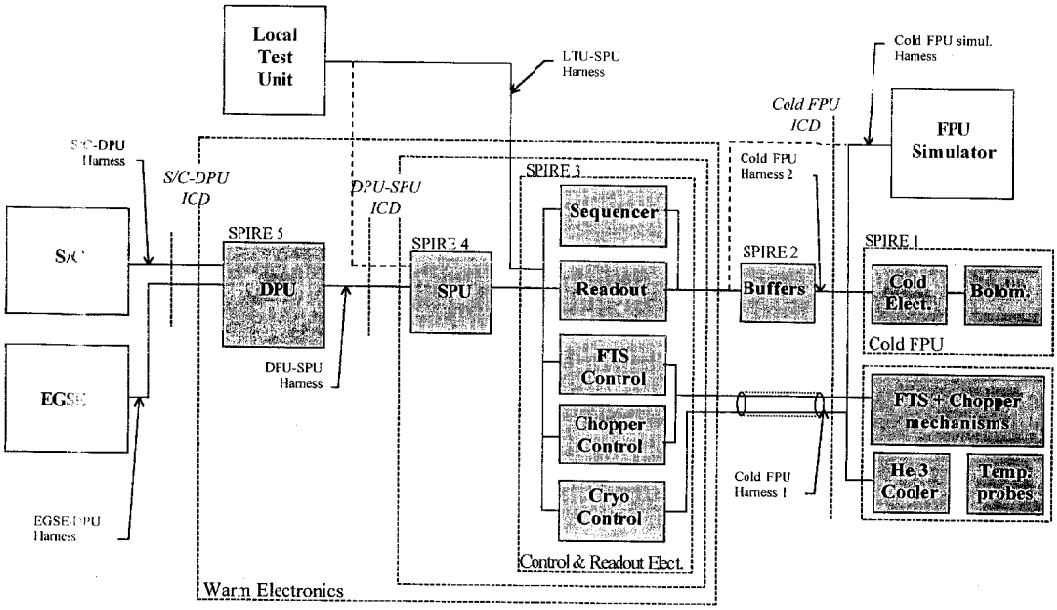
Chairman: Morning – Ken King

Afternoon - Colin Cunningham

9:00	Introduction and aims of meeting	Matt
9:05	Agree Agenda	Colin
9:15	Warm Electronics Architecture	Louis
9:30	Review of options	Jean-Louis
10:30	Draw up table of pros & cons	
10:45	Agree recommendation	Matt
11:15	Models vs. part grade	Louis
11:30	Reliability	Louis
	Risk analysis philosophy	Louis
	Redundancy – Science drivers	Matt
12:30	LUNCH	
13:30	Overall Opto-mechanical systems design	Bruce
13:50	FTS systems design	Bruce
14:00	Thermal system design - Plan for PDR	Colin
14:10	Telescope Interface – What is missing from the IID-B for the July ESTEC meeting?	Colin
14:20	Interaction with AOCS (Esp. peak-up)	Matt
14:30	Wiring and Connectors – requirements for IRD	Colin
14:45	Thermal and Mass Budgets	Colin
15:00	Instrument Requirements Document Review	Bruce
15:30	Instrument Development Plan Review	Ken
16:30	Interface Control Plan Review	Colin
17:00	Review Actions from this and previous meetings	Colin
17:15	Review Aims of Meeting	Colin
17:30	Close	

FIRST/SPIRE

Electronics Block Diagram



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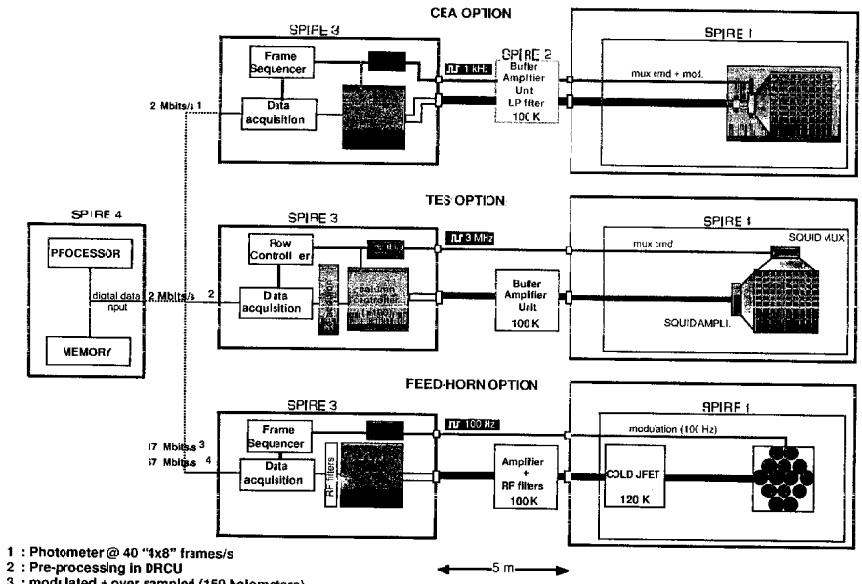
WARM ELECTRONICS CONFIGURATION vs DETECTOR OPTION



1 : Photometer @ 40 "1x8" frames/s
2 : Pre-processing in DRCU
3 : modulated + over sampled (150 bolometers)
4 : " " (500 bolometers)

17/05/99

FIRST/SPIRE

LIST OF QUESTIONS

- SPECTROMETER DATA PROCESSING

  • DECIMATION / CONVOLUTION : DETAILS
  • SAMPLING RATE : UP TO 200 / S
  • POST-SPU DATA RATE

- GSFC ELECTRONICS INTEGRATION

  • FPGA : RELIABILITY ASPECT (144 FPGA TOTAL X 100 PINS !)
  • FPGA POWER CONSUMPTION : REALLY SO LOW ?
  • FPGA → ASIC : TO BE ANALYSED
  • MORE DETAILED FUNCTIONNAL DIAGRAM (WITH BUS WIDTH+FREQUENCY) FOR GATE NUMBER ESTIMATION USING VHDL DESCRIPTION
  • RELATION BETWEEN PRIMARY FRAME RATE AND ADC SAMLING RATE

- JPL ELECTRONICS

  • DATA PROCESSING : FILTERING / DEMODULATION
  • DEMODULATION IN HARDWARE
  • CEA/SAP : A→D CONVERTER (16-BITS OR MORE) FOR SPACE APPLICATION STUDY STARTED

- PHOTOMETER DATA PROCESSING

  • POST-SPU DATE RATE IN BEAM STEERING MODE

- CHOPPER DESIGN

  • WHO DESIGN WHAT (MECHANISM / ELECTRONICS) ?

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FIRST/SPIRE

SPIRE DETECTOR READOUT INTERFACING (1)

• PHOTOMETER : CURRENT FRAME RATE IS 40 Hz (DERIVED FROM FTS CONSTRAINTS)

NEW : THIS FRAME RATE IS REDUCED TO 10 Hz BY CO-ADDING 4 SUCCESSIVE FRAMES (SEE "SPIRE DATA RATE" NOTE FROM MG & BS) IN BOTH CHOP AND BEAM STEERING MODES.

1- FOR GSFC/NIST OPTION SINCE PRIMARY FRAME RATE IS 20000/S CO-ADDITION IS ALREADY FORESEEN AT THE ANALOG SIGNAL PROCESSING ELECTRONICS LEVEL :

→ POSSIBILITY TO CO-ADD 2000 FRAMES DIRECTLY TO OBTAIN A 10 Hz FRAME RATE ?
→ FRAME ACCUMULATION IS TRIGGERED BY AN EXTERNAL PULSE SIGNAL (E.G. FROM STEERING MIRROR CONTROLLER)
→ ROW CONTROLLERS SHALL GENERATE A *FRAME READY* PULSE WHEN A CO-ADDED FRAME IS READY FOR TRANSFER TO SPU OR DPU

2- FOR CEA OPTION SIGNAL INTEGRATION IS PERFORMED TO ACHIEVE A 40 Hz FRAME RATE :

→ POSSIBILITY TO REDUCE DOWN TO 10 Hz HAS TO BE EVALUATED
→ FRAME READOUT IS TRIGGERED BY AN EXTERNAL PULSE SIGNAL (SAME AS ABOVE)
→ DETECTOR SEQUENCERS SHALL GENERATE A *FRAME READY* PULSE WHEN FRAME IS READY FOR TRANSFER TO SPU OR DPU

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3- FOR JPL OPTION FRAME RATE IS 7000/S DUE TO LARGE OVER SAMPLING (SEE FAX .. FROM JB) :

→ SPU IS PROBABLY NOT ABLE TO HANDLE CONTINUOUS DATA FLOW
→ POSSIBILITY TO INTRODUCE DATA PRE-PROCESSING IN THE ANALOGUE SIGNAL PROCESSING ELECTRONICS TO BE ANALYSED (SEE PROPOSAL)
→ BOLOMETERS MODULATION SHALL PROBABLY BE SYNCHRONISED WITH CHOPPER MOTION
→ CLOCK GENERATOR SHALL GENERATE A *FRAME READY* PULSE WHEN FRAME IS READY FOR TRANSFER TO SPU OR DPU

• SPECTROMETER

NEW : DOCUMENT "BASELINE FTS OPERATING PARAMETERS" FROM BS GIVES THE FOLLOWING FRAME RATES FOR AN OVER SAMPLING FACTOR OF 5 :

- 133 Hz FOR 12x12 ARRAY
- 200 Hz FOR 16x16 ARRAY

COMMENT : DO WE REALLY NEED 2 DIFFERENT FRAME RATES ?

• GSFC OPTION : NO SPECIFIC PROBLEM - PRIMARY FRAME ACCUMULATION IS ADAPTED TO THIS FRAME RATES (RESPECTIVELY 150 & 100 FRAMES HAVE TO BE ACCUMULATED).

SPIRE DETECTOR READOUT INTERFACING (3)

→ FRAME ACCUMULATION IS TRIGGERED BY AN EXTERNAL PULSE SIGNAL (FROM FTS MIRROR CONTROLLER)
→ ROW CONTROLLERS GENERATE A *FRAME READY* PULSE WHEN A CO-ADDED FRAME IS READY FOR TRANSFER TO SPU OR DPU

• CEA OPTION : SIGNAL INTEGRATION HAS TO BE REDUCED (SPECTROMETER ANALOGUE ELECTRONICS IS NO MORE IDENTICAL TO PHOTOMETER).

→ IMPACT ON CONCEPT & POWER CONSUMPTION TO BE ANALYSED
→ SYNCHRONISATION CONCEPT AS FOR PHOTOMETER

• JPL OPTION : 100 Hz MODULATION MAY BE INCOMPATIBLE WITH SUCH FRAME RATES

→ POSSIBILITY TO INCREASE MODULATION FREQUENCY TO BE ANALYSED

SPIRE Analog Signal Processing Output Rates (JPL Option)

Photometer :

Focal Plane Configuration	Number of pixels	Pixel Sampling Rate (Hz)	Number of Bits	Data Rate (16-bit words/s)	Data Rate (Mbits/s)
FOV = 4 x 4 2.3λ feed-horn	117	7000	16	$0.8\ 10^6$	13.1
FOV = 4 x 8 1.7λ feed-horn	468	7000	16	**$3.3\ 10^6$**	52.4

• Even if DRCU and SPU interface by parallel data transfer (16-bit words) the data rate of the "468 pixels" option should be difficult to handle with a microprocessor clocked at 10 or 20 MHz (even if it's a DSP !).

➔ DATA RATE REDUCTION (IN THE DRCU) IS HIGHLY RECOMMENDED !

Solutions to be investigated :

☐ **Reduction of the over sampling (in that case the demodulation is still implemented by software)**

☐ **Demodulation is performed analogically by the analog signal processing**

☐ **Demodulation is performed digitally by hardware (based on FPGA - see proposal) by the analog signal processing**

THE ERC32 PROCESSOR (I)

• ERC32 IS AN EUROPEAN PROJECT FOR DEVELOPING A 32-BIT PROCESSOR COMPATIBLE WITH SPARC V7 FOR SPACE APPLICATIONS

• THIS PROGRAM INVOLVES :
- ESA
- TEMIC
- MATRA MARCONI SPACE
- SES (SAAB)
- ...

• A CHIP SET IS CURRENTLY AVAILABLE FROM TEMIC IN RAD-TOLERANT (UP TO 40 KRAD) VERSION

• MONOCHIP VERSION IS PLANNED BY END OF 99 (SPACE GRADE)

→ MATRA MARCONI SPACE HAS DESIGNED THE "COMMON PROCESSOR BOARD" FOR THE COLUMBUS PROGRAMME

THIS BOARD INCLUDES :
- TEMIC ERC32 CHIP SET
- 2, 4 OR 8 MBYTES OF EDAC PROTECTED STATIC RAM
- 1, 2, 3 OR 4 MBYTES OF FLASHPROM
- CLOCK & WATCHDOG GENERATOR
- INTERRUPT CONTROLLER
- VME INTERFACE / SERIAL INTERFACES

PERFORMANCES :
- 9 MIPS / 2 MFLOPS @ 14 MHz

THE ERC32 PROCESSOR (2)

OPERATING SYSTEM : - Real Time OS32 BASED ON VxWORKS (FROM WIND RIVER SYSTEMS)

TYPICAL POWER CONSUMPTION : 10 W

BOARD IS AVAILABLE IN 3 VERSIONS :
- PROTOTYPE (FOR SOFTWARE DEVELOPMENT)
- ENGINEERING MODEL
- FLIGHT MODEL

• A PRELIMINARY ANALYSIS (BASED ON MMS DATA) SHOWS THE BOARD IS COMPLIANT WITH SPIRE RADIATION ENVIRONMENT (TBC)

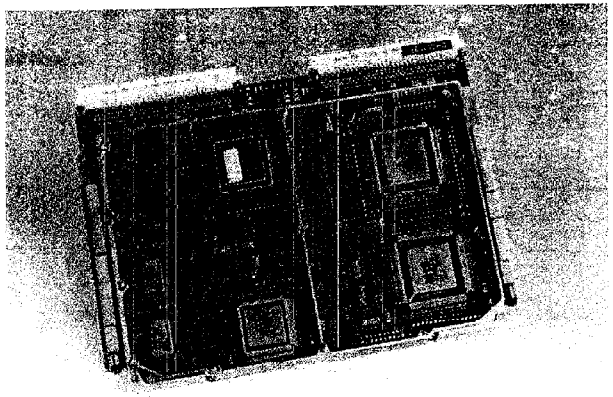
• STANDARD EEE PART QUALITY : MIL-B (INSTEAD OF SCC B)

• COST :
- 500 KF FOR MIL-B COMPONENT GRADE
- 1.1 MF FOR HI-REL COMPONENT GRADE

→ THE PROBLEM OF EEE PART QUALITY HAS TO BE DISCUSSED WITH ESA IN ORDER TO DEFINE AN ACCEPTABLE INTERMEDIATE QUALITY LEVEL

MATRA MARCONI SPACE

COMMON PROCESSOR BOARD



MATRA MARCONI SPACE developed in the frame of the COLUMBUS programme a Common Processor Board (CPB). This board is a VME board which provides the central processing capability to on-board computers for space applications.

The CPB is based on a SPARC™ architecture. It is typically used as the slot 1 system controller of a VME computer but can also be configurated to operate as a VME master for multiprocessing applications.

Its RAM is protected by Error Detection And Correction. The FlashPROM includes a boot firmware and can be user-programmed to store additional application software. The CPB can be provided with different RAM/PROM configurations

The CPB is supported by a commercial off-the-shelf real-time POSIX operating system with a C and Ada cross-development environment.

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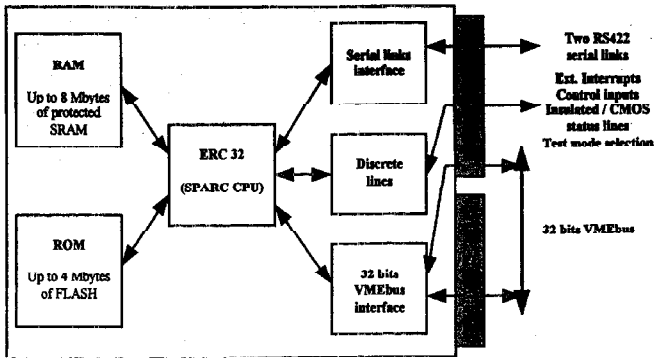
MATRA MARCONI SPACE



CPB Block diagram

TECHNICAL FEATURES

Microprocessor	:	Radiation tolerant ERC32 chip set, compatible with SPARC™ v7
Memory	:	2, 4 or 8 Mbytes SRAM protected by EDAC 1, 2, 3 or 4 Mbytes FlashPROM
Performance	:	9 MIPS Integer / 2 MFLOPS
VME Interface	:	IEEE/ANSI std 1014-1987 compliant VME system controller : master, power monitor, bus timer, interrupt handler, bus arbiter, IACK daisy-chain driver. Supports A24:A16 / D32:D16:D8 data transfer modes.
Serial Interface	:	2 x EIA-RS-422 serial ports (9600 bps)
Operating system	:	Real time OS32, based on vxWorks™ v5.3.1
Software development environment	:	Tornado™ v1.0.1
Power	:	+5V, typ. 2A / +12V, typ 0.04A (for FlashPROM reprogramming)
Mechanical	:	6U VME conduction cooled board
Mass	:	< 600g
EEE part quality level	:	MIL-B or equivalent
Reliability	:	Failure rate < 6000 fits (MIL-HDBK-217F, Notice 1, SF environment, average PCB temperature = 55°C)

OCTOBER 1998
Subject to change without notice

SYSTEM REDUNDANCY PHILOSOPHY: WARM ELECTRONICS

- **BUFFER AMPLIFICATION UNIT OR JFET BOX:**
  Thermometers, biases. , heaters . | double wires!
- **DRCU**
  - **PHOTOMETER ARRAYS:**
    Analog Signal processing boards NON REDUNDANT. Frame sequencer ?
  - **SPECTOMETER ARRAYS:**
    Analog Signal processing boardsNON REDUNDANT. Frame sequencer?

    ↑ Redundancy ↓
  - **CHOPPER MECHANISM BOARD:**
    Two units fully redundant in one board biases
  - **FTS MECHANISM BOARD:**
    Two units fully redundant in one board biases
- **SPU**
  fully redundant in two boards
- **DPU**
  fully redundant in two boards
  - **THERMOMETRY:**
  - **SHUTTER MECHANISM:**
  - **PHOTOMETER CALIBRATION SOURCE :**
  - **SPECTROMETER CALIBRATION SOURCE:**

interfaces? addressed note subsystem

SYSTEM REDUNDANCY PHILOSOPHY: FOCAL PLANE UNITS

- **THERMOMETRY:** Cooler (2), Focal plane 300 mK (5), Calibration sources (2), chopper & FTS mechanism (2), 2 K stage, 4 K stage. ← 2 sensors + 4 wires. (8 wires. / 4 wires)
- **COOLER** Charcoa pumpheater thermal switches heaters(2)
- **PHOTOMETER ARRAYS:** Biases, clocks ,signals. ➡ double segment circuits
- **SPECTOMETER ARRAYS:** Biases, clocks ,signals. ″
- **CHOPPER MECHANISM:** Drive Power, position sensors → safe dead. position!
- **FTS MECHANISM:** Drive power, position sensor (FTS sampling) → safe redundancy.
- **SHUTTER MECHANISM:** Actuator power, release sensor Zind. coils in the mech..
- **PHOTOMETER CALIBRATION SOURCE :** Source power wires doubled.
- **SPECTROMETER CALIBRATION SOURCE:** source power (f compensation) (diff volore sources.)

SYSTEM REDUNDANCY PHILOSOPHY: WARM ELECTRONICS

- BUFFER AMPLIFICATION UNIT OR JFET BOX:
  Thermometers, biases.

- DRCU
  - **PHOTOMETER ARRAYS:**
    Analog Signal processing board: NON REDUNDANT, Frame sequencer ?
  - **SPECTOMETER ARRAYS :**
    Analog Signal processing boardsNON REDUNDANT, Frame sequencer?
  - **CHOPPER MECHANISM BOARD:**
    Two units fully redundan. in one board biases
  - **FTS MECHANISM BOARD:**
    Two units fully redundan. in one board biases

- SPU
  fully redundant in two boards

- DFU
  fully redundant in two boards

  - **THERMOMETRY:**
  - **SHUTTER MECHANISM:**
  - **PHOTOMETER CALIBRATION SOURCE :**
  - **SPECTROMETER CALIBRATION SOURCE:**

SYSTEM RISK ANALYSIS: FOCAL PLANE UNITS

-THERMOMETRY:
Cooler (2), Focal plare 300 mK (5), Calibration sources (2), chopper & FTS mechanism (2), 2 K stage, 4 K stage.

-COOLER:
Charcoa pump heate-, thermal switches heaters(2)

-PHOTOMETER ARRAYS:
B ases, clocks ,signals.

-SPECTOMETER ARRAYS:
Biases, clocks ,signals.

-CHOPPER MECHANISM:
Drive Power, position sensers

-FTS MECHANISM:
Drive power, position senser (FTS sampling)

-SHUTTER MECHANISM:
Actuator power. release sensor (opened in space ?)

-PHOTOMETER CALIBRATION SOURCE :
Source power

-SPECTROMETER CALIBRATION SOURCE:
source power (if compensation)

HIGH

LOW

Dev Risk	OPTION A	OPTION C
I/Fs		Less I/Fs (Electrical) (Mechanical)
Accuracy		
S/W Dev	Data Processing (FFT) may be easier	S/w developed by 1 group Common tools for GPU/DRCV S/W Knowledge of S/W tools already available General Purpose Processor
Int & Test		2 units to integrate rather than 3 (less EGSE / Sims) - lower risk
Resources	Possibly Faster (built-in FFT)	Frees some resources (mass power)
Reliability		Less cards required less I/Fs Qualified for ISS Easier redundancy
Management		1 less group involved

Introduction

In this note the order of the optical components in each of the instrument channels (photometer and spectrometer) is given and naming convention for the optical components is proposed (tables 2 and 3). A mass estimate is given in the form of a spread sheet tabulation (table 3) and the topological distribution of the elements of the instrument hardware is shown for the photometer (figure 1) and spectrometer (figure 2).

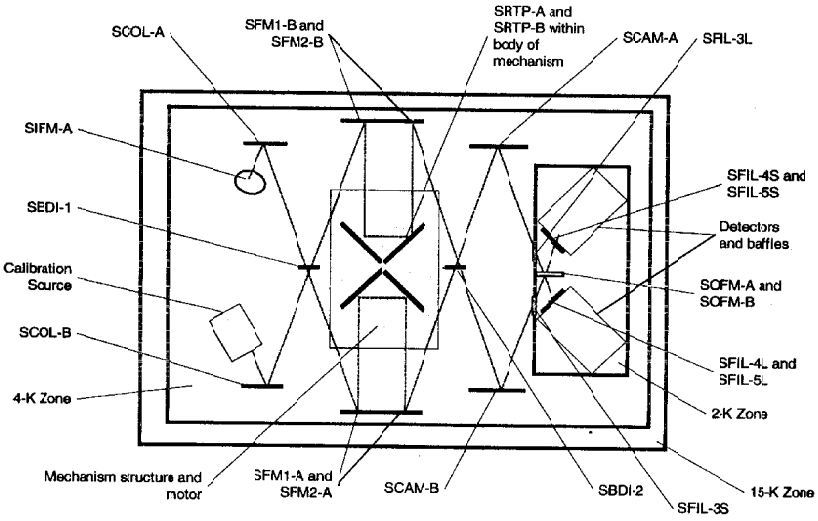
Tabulation of SPIRE optical elements

Notes:

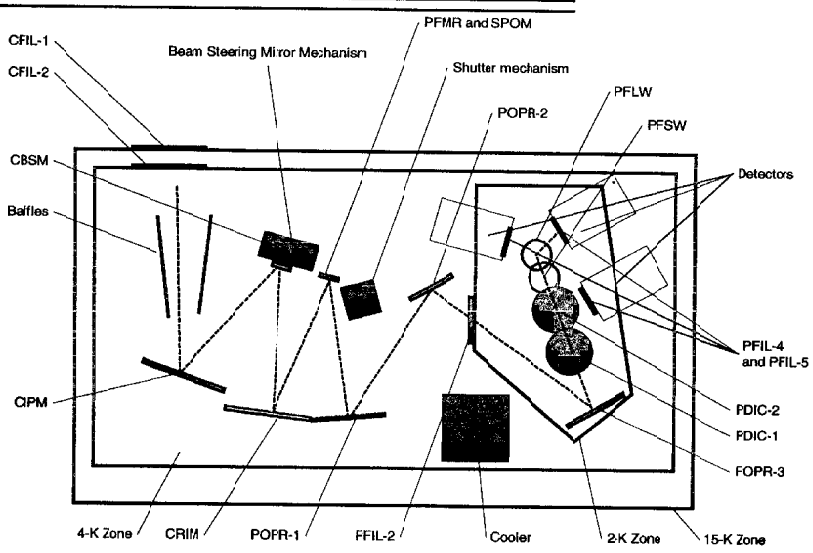
- All components in the optical chain are given a four-letter code, with additional characters to designate multiple components of the same type.
  - First letter C ⇒ Common component (used by both photometer and spectrometer)
  - First letter P ⇒ Photometer component
  - First letter S ⇒ Spectrometer component

- Photometer arrays:
  - SW ≡ 250 μm array
  - MW ≡ 350 μm array
  - LW ≡ 500 μm array

- Spectrometer arrays:
  - Band S ≡ 200-300 μm array
  - Band L ≡ 300-670 μm array



Topological layout of mass on "spectrometer" side of SPIRE instrument - read in conjunction with spreadsheet.
Figure 2



Topological layout of mass on "photometer" side of SPIRE instrument - read in conjunction with spreadsheet and filter table.
Figure 1

Order of optical elements in the SPIRE photometer			
Number	**Component ID**	**Temp (K)**	**Description**
1	CFIL-1	11	Input filter on 11-K box
2	CFIL-2	4	Edge filter over entrance to 4-K box
3	CIPM	4	Common instrument input mirror
4	CBSM	4	Common mirror at pupil (Beam Steering Mirror)
5	CRIM	4	Common reimaging mirror
6	PFMR	4	Field mirror
7	POPR-1	4	Optical relay input mirror
8	POPR-2	4	Optical relay second mirror
9	PFIL-3	2	Edge filter at 2-K box entrance (pupil)
10	POPR-3	2	Optical relay output mirror
11	PDIC-1	2	First dichroic (reflects $\lambda >$ TBD μm)
12	PDIC-2	2	Second dichroic (reflects $\lambda >$ TBD μm)
13	PFLW	2	Plane fold mirror for LW array
14	PFSW	2	Plane fold mirror for SW array
15	PFIL-4S, PFIL-4M, PFIL-4L	0.3	Bandpass filters over SW, MW or LW arrays
16	PFIL-5L, PFIL-5M, PFIL-5L	0.3	Blocker filters over SW, MW or LW arrays

Table 1: Order and nomenclature for photometer optical components

Order of optical elements in the SPIRE FTS			
Number	**Component ID**	**Temp (K)**	**Description**
1	CFIL-1	11	Input filter on 11-K box
2	CFIL-2	4	Edge filter over entrance to 4-K box
3	CIPM	4	Common instrument input mirror
4	CBSM	4	Common mirror at pupil (Beam Steering Mirror)
5	CRIM	4	Common reimaging mirror
6	SFOM	4	Spectrometer field pick-off mirror
7	SIFM-A or SIFM-B	4	Input Fold mirror in arm A or B
8	SCOL-A or SCOL-B	4	Collimator for arm A or B
9	SBDI-1	4	Beam divider 1 (common to both arms)
10	SFM1-A or SFM1-B **	4	First Fold mirror in arm A or B
11	SRTP-A or SRTP-B **	4	Roof-Top mirror in arm A or B
12	SFM2-A or SFM2-B	4	Second Fold mirror in arm A or B
13	SBDI-2	4	Beam divider 2 (common to both arms)
14	SCAM-A or SCAM-B	4	Camera mirror in arm A or B
15	SFIL-3S or SFIL-3L	2	2-K filters at entrance to 2-K box (pupil)
16	SOFM-A or SOFM-B	4	Output Fold mirror in arm A or B
17	SFIL-4S or SFIL-4L	0.3	Bandpass filters over Band S and Band L arrays
18	SFIL-5S or SFIL-5L	0.3	Blocking filters over Band S and Band L arrays

Table 2: Order and nomenclature for spectrometer optical components

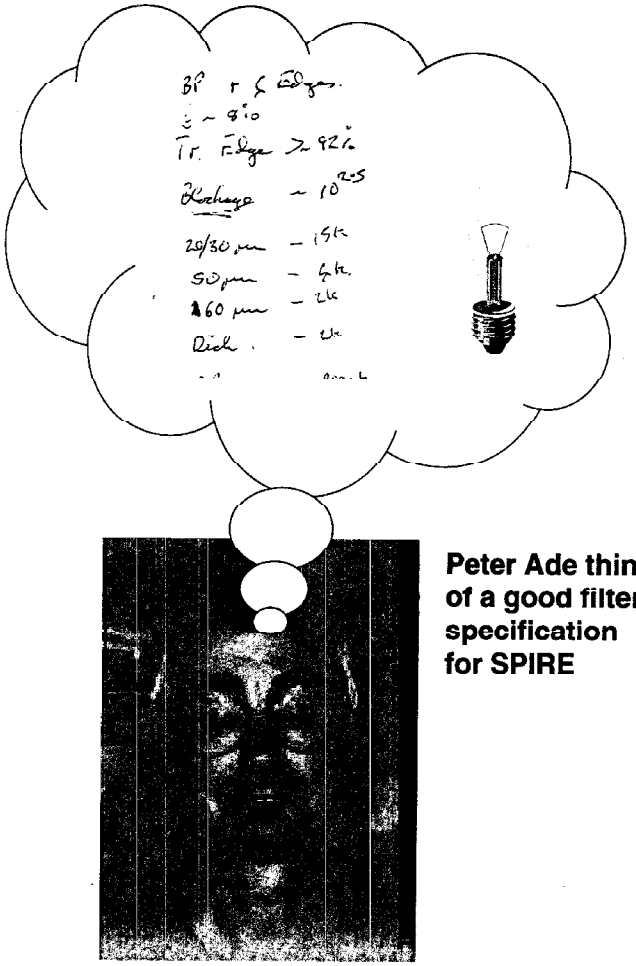
Mass estimate of new photometer spectrometer layout using mirror sizes+20% and aspect ratio of 6:1 for small mirrors and 12:1 for big ones.

Photometer Hardware:								
Mirrors	**Est. Mass**	**Temp**	Size y or Diam	Size z	Area (cm2)	Volume (6:1)	Raw Mass	Adopted Mass
CIPM (M3)	212	4	132	54	71.28	156.816	423.4032	212
CBSM (M4)	12	4	32		8.042477	4.28932117	1..58117	12
CRIM (M5)	496	4	161	85	136.85	367.2141667	991.4783	496
PFMR (M6)	32	4	51	27	13.77	11.7045	3..60215	32
POPR-1 (M7)	313	4	118	100	118	232.0666667	626.53	313
POPR-1 (M8)	75	4	60		28.27433	28.27433389	76.3407	76
POPR-3 (M9)	315	2	112	112	125.44	234.1546667	632.2175	316
PFLW (Fold)	97	2	60	60	36	35	97.2	97
PFSW (Fold)	97	2	60	60	36	35	97.2	97
Filters								
CFIL-1	50	15						
CFIL-2	50	4						
PFIL-3	50	2						
PDIC-1	50	2						
PDIC-2	50	2						
Detectors								
3 arrays	1500	2						
Thermal Straps								
4-K	300	4						
2-K structure	300	2						
2-K cooler	300	2						
Cooler								
Cooler	500	4						
Thermal Straps	500	2						
Baffles								
4-K Baffles	500	4						

2-K Baffles	200	2						
Harness								
Array Harness 800	400	4						
The rest of the harness 200	100	4						
Chopper								
BSM Mech/structure	500	4						
Shutter								
Shutter mech and mount	200	4						
Total Phot.	7201							
Spetrometer hardware:								
Mirrors	**Est. Mass**	**Temp**	Size y or Diam	Size z	Area (cm2)	Volume (6:1)	Raw Mass	Adopted Mass
SPOM	7	4	22	30	6.6	2.42	6.534	7
SIFM-A	32	4	45		15.90431	11.92823461	32.20623	32
SCOL-A	168	4	78		47.78362	62.11871155	167.7205	168
SCOL-B	168	4	78		47.78362	62.11871155	167.7205	168
SFM1-A and SFM2-A	89	4	60	55	33	33	89.	89
SFM1-B and SFM2-B	89	4	60	55	33	33	89.	89
SRTP-A	95	4	42	120	50.4	35.28	95.256	95
SRTP-B	95	4	42	120	50.4	35.28	95.256	95
SCAM-A	168	4	78		47.78362	62.11871155	167.7205	168
SCAM-B	168	4	78		47.78362	62.11871155	167.7205	168
Filters								
SBDI-1	50	4						
SBDI-2	50	4						
SFIL-3S	50	2						
SFIL-3L	50	2						
Detectors								
2 arrays	600	2						
Baffles								
2-K Baffles	200	2						
Mechanism								

Structure	400	4						
Motor	500	4						
Calibration source								
Source and mount	200	4						
Total Spectrometer	3178							
Total Hardware	10379.1							
Total with cont.	12455							
Covers:	x	Y	z		**Thick**	**Mass**		
Area 2-K	25	25	35	4750	0.1	1283		
Area 4-K	43	38	66	13960	0.1	3769		
Area 15-K	44	41	69	12509	0.01	338		
Total HW+Covers	15769				**4-K Mass**			**2-K Mass**
With contingency	18922			**Phot 4K**	3740	**Phot 2K**		3460
				Spect 4K	2328	**Spect 2K**		900
JFET Box (300 dets)	2000			**Total HW 4K**	6068	**Total HW 2K**		4360
With contingency	2400			**Total HW + Cover**	9837	**Total HW +cover**		5643
				Total with cont.	11805			6771
What we told ESA	34000							
With contingency	40800							
Structure Alloc.	16231							
With contingency	19478							

Table 3: Spread sheet for mass estimates



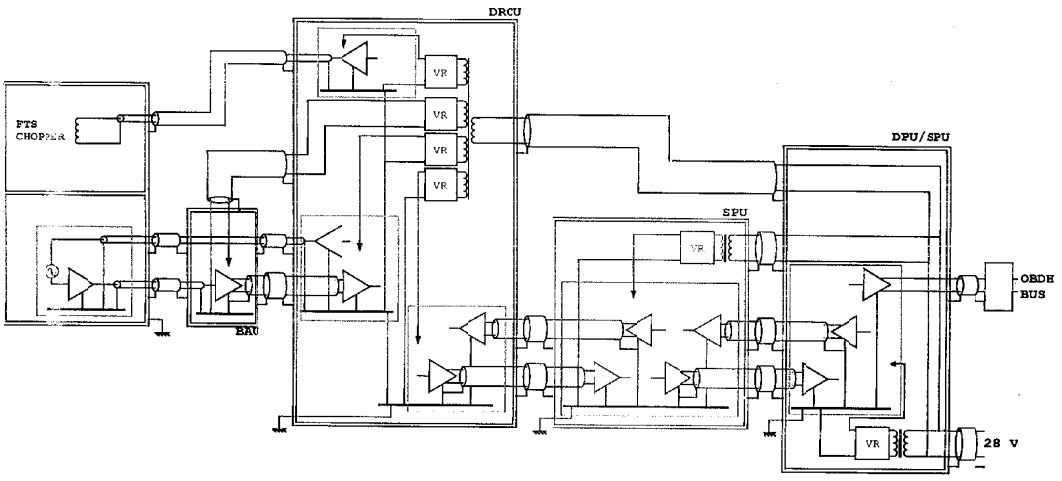
Peter Ade thinks of a good filter specification for SPIRE

C.R. CUNNINGHAM

GAPS in the IID-B

1) MECHANICAL INTERFACE DWG.
   MSSL 1st STAGE 27 MAY
2) ALIGNMENT & STABILITY REQUIREMENTS
   LAS 1st STAGE 27 MAY
3) THERMAL MODEL
   CRC, BRUCE, MATT 27 MAY
4) WARM ELECTRONICS POWER (150W!)
   MATT EMAIL T. PANSOGEL
5) GROUNDING & BONDING
   VALIDATION OF DESIGN
6) ATTITUDE & ORBIT CONTROL/POINTING
7) EMC & FREQUENCY PLAN
   DRAFT DETECTOR GROUPS MID JUNE
   COMMENT ON CBA GROUNDING PLAN "
8) EGSE, MGSE, OGSE
   NOTES BY KEN, MSSL, RUTHERFORD MID JUNE
9) BAU THERMAL DESIGN & MODEL
   GSFC BY MID JUNE

SPIRE GROUNDING DIAGRAM



24/03/99

5.9.1.2 Thermal table FSFPU

There are presently 3 versions under consideration.

5.9.1.2.1 CEA and GSFC arrays (4x4 or 4x8 arcminutes FOV)

Temp. Stage	Item	CEA/TES			
		Standby	OFF	PHOT	SPEC
"15-K"**		0	0	0	0
"4-K"*	Wires	1.1	1.1	1.1	1.1
	Radiation	0.6	0.6	0.6	0.6
	Mechanisms	0.0	0.0	2.0	7.4
	Structure	2.0	2.0	2.0	2.0
	Total	3.7	3.7	5.7	11.1
"2-K"***	Wires	0.1	0.1	0.1	0.1
	Dissipation	2.0	0.0	2.0	2.0
	Cooler	1.0	1.0	1.0	1.0
	Structure	1.0	1.0	1.0	1.0
	Total	4.1	2.1	4.1	4.1

Note: 'Standby' with detectors and cold read-out on, ready to start observation, but mechanisms stopped.

5.9.1.2.2 Feed-horn array (150 bolometers, 4x4 arcminutes FOV)

Temp. Stage	Item	Feedhorn (150 dets)			
		Standby	OFF	PHOT	SPEC
"16 K"**	JFET Box	20	0	20	5
"4-K"*	Wires	1.1	1.1	1.1	1.1
	Radiation	0.6	0.6	0.6	0.6
	Mechanisms	0.0	0.0	2.0	7.4
	Structure	2.0	2.0	2.0	2.0
	Total	3.7	3.7	5.7	11.1
"2-K"***	Wires	0.1	0.1	0.1	0.1
	Dissipation	0.0	0.0	0.0	0.0
	Cooler	1.0	1.0	1.0	1.0
	Structure	1.0	1.0	1.0	1.0
	Total	2.1	2.1	2.1	2.1

Either Photometer or Spectrometer JFETS are switched on in STANDBY mode, and switched off in OFF mode. Average power in OBSERVING mode can be calculated assuming JFETS for photometer can be turned off when spectrometer is in operation, and vice versa.
4 K heatloads assume 15 K level is 11K

** Excludes conducted and dissipative heatloads from cryo harness connecting to 300 K level.

5.9.1.2.3 Feed-horn array (300 bolometers, 4x8 arcminutes FOV)

Temp. Stage	Item	Feedhorn (300 dets)			
		Standby	OFF	PHOT	SPEC
"15-K"**	JFET Box	40	0	40	10
"4-K"	Wires	1.1	1.1	1.1	1.1
	Radiation	0.6	0.6	0.6	0.6
	Mechanisms	0.0	0.0	2.0	7.4
	Structure	2.0	2.0	2.0	2.0
	Total	3.7	3.7	5.7	11.1
"2-K"**	Wires	0.1	0.1	0.1	0.1
	Dissipation	0.0	0.0	0.0	0.0
	Cooler	1.0	1.0	1.0	1.0
	Structure	1.0	1.0	1.0	1.0
	Total	2.1	2.1	2.1	2.1

Either Photometer or Spectrometer JFETS are switched on in STANDBY mode, and switched off in OFF mode. Average power in OBSERVING mode can be calculated assuming JFETS for photometer can be turned off when spectrometer is in operation, and vice versa.
4 K heatloads assume 15 K level is 11K

** Excludes conducted and dissipative heatloads from cryo harness connecting to 300 K level.

*** Includes dissipation of ^{3}He refrigerator when operating. Recycle mode dissipates 90 mW (TBC) for 2 out of every 48 hours.

5.9.1.3 Thermal Model FSBAU

TBD. Thermal design of the BAU is ESA responsibility.(TBC)**Thermal Table FSBAU**

TBD

5.9.2 Outside cryostat

Project code	Instrument unit	Power dissipation (W)
FSBAU	Buffer Amplifier Unit	2.5 (TBD) *

* Average may be lower if thermal and electronic design allows it to be switched off when inactive.

5.9.3 On SVM

The table below shows the heat dissipation of the units mounted on the SVM:

STATUS OF IRD

SYSTEMSTEAM
13/5/99 CALTECH

2. INSTRUMENT OVERVIEW + TOP LEVEL (SRD)
   REQS WRITTEN AS DRAFT

3. MODEL PHILOSOPHY + QUAL REQS IN DRAFT
   ~~ASSY~~ VERIFICATION REQS NOT WRITTEN
   SAFETY REQS NEED WORK
   AUTONOMY REQS NOT WRITTEN
   RELIABILITY + ~~REDUNDANCY~~ NEEDS WORK
   EMC NOT WRITTEN — REDUNDANCY PHILOSOPHY
   * ~~FLIGHT~~ OPS SKETCHED IN — NEEDS DETAILING
     ~~INSTRUMENT~~

4. GLOBAL BUDGETS NEED INPUTTING
   COMMON STRUCTURE IN DRAFT
   ^3He IN DRAFT
   SHUTTER NOT INPUT — DOC EXISTS
   HARNESS NEEDS WORK
   PHOTOMETER — ALL SUBSYSTEMS **REQS IN DRAFT**
   SPECTROMETER — DETECTORS NEEDS INPUTTING
   CAL SOURCE NEEDS INPUTTING

5. ~~WARM~~ ELECTRONICS
   ⇒ SEPARATE DOCUMENT DISTRIBUTED BY JLA

6. ~~AIV PAD~~ — NOT STARTED

SPIRE Instrument Development Plan

- **Purpose:**
  - *What is being Developed?*
    - Instrument models
    - Instrument Breakdown to subsystems
    - Subsystem development
  - *How is it being Verified ?*
    - Subsystem Verification
    - Instrument Verification
    - Test Facilities
  - *When will it be provided*
    - ESA Schedule
    - SPIRE Schedule
  - *How will it be operated*

SPIRE Instrument Development Plan

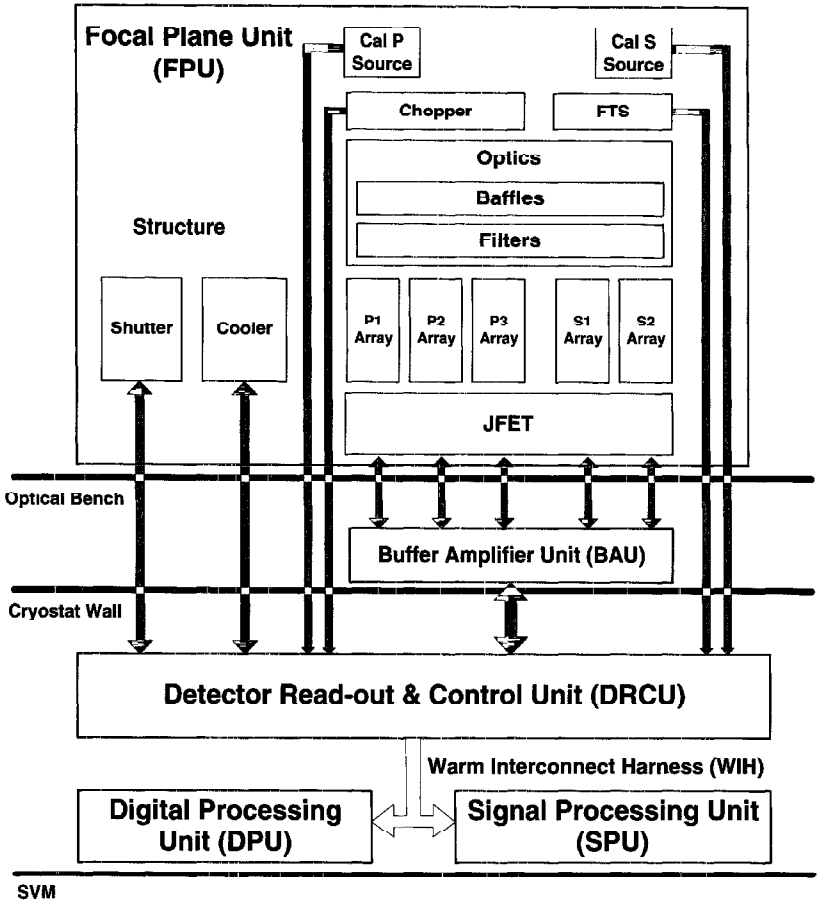
- **Instrument Models**
  - *Development Models*
    - FPU: CQM, PFM, FS
    - WE: EM, AVM, CQM, PFM, FS parts
  - *Deliverable Models*
    - AVM, CQM, PFM, FS (FPU + WE Parts)
- **Instrument Breakdown**
- **Subsystem Development**
  - *Follows IDP sections:*
    - Models, Breakdown
    - Qualification, AIT
    - Schedule

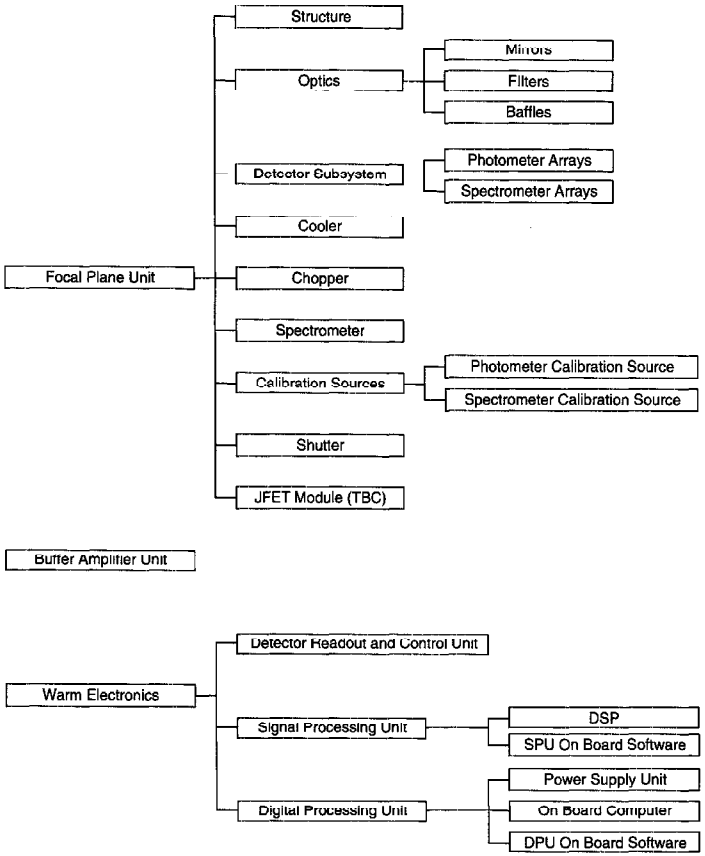
Products & Tests vs. Models (1)

		Resp.	EM	AVM	CQM	PFM	FS	Comments
WE UNITs								
DPU								
	Electronics							
	CPU Board	IFSI	1	1	2	2	(2/3)	FS shared with other Inst.
	Memory	IFSI	1	1	2	2	(2/3)	
	Power Supply	IFSI	1	1	2	2	(2/3)	
	Component Grade		Std	Std	Ext	Qual	Qual	
	Mechanics							
	DPU Box	IFSI	1	1	1	1	(1/2)	FS shared with other Inst.
	Connectors	IFSI	X	X	X	X	X	
	S/W							
	LL s/w	IFSI	V0	V1	V2	V flight	V flight	
	HL s/w	IFSI	V0	V1	V2	V flight	V flight	
SPU								
	H/W							
	CPU Board	IAC	1	1	2	2	1	
	Memory	IAC	xMo	xMo	2*(xMo)	2*(xMo)	xMo	
	Power Supply	IAC	1	1	2	2	1	
	Component Grade		Std	Std	Ext	Qual	Qual	
	Mechanics							
	SPU Box	IAC	1?	1	1	1	(1/2)	FS shared with other Inst.
	Connectors	IAC	X	X	X	X	X	
	S/W							
	LL s/w	IAC	V0?	V1?	V2?	V flight	V flight	
	HL s/w	SAp	V0?	V1?	V2?	V flight	V flight	
DRCU								
	Electronics							
	Detector Readout	SAp	1	-	1	1	1	
	FTS Control	LAS	1	-	2	2	1?	
	Cryo Control	SAp	1	-	2	2	1?	
	Chopper Control	SAp	1	-	2	2	1?	
	Calib. Source Control	SAp	1	-	2	2	1?	
	H/K readout	SAp	1	-	2	2	1?	
	Component Grade		Std	-	Mil	Qual	Qual	
	Mechanics							
	DRCU Box	SAp	1	-	1	1	1	
	Connectors	SAp	X	X	X	X	X	
BAU								
	Electronics							
	Buffers	SAp	1		1	1	1	
	Temp. Regulation	SAp	1		1	1	1	
	Component Grade		Std		Mil	Qual	Qual	
	Mechanics							
	BAU Box	SAp	1	2	2	2	1	
	Connectors	SAp	X	X	X	X	X	
Harness								
	DPU to SPU	SAp	1	1	2	2	1	
	SPU to DRCU	SAp	1	1	2	2	1	
	DRCU to BAU	SAp	1	-	2	2	1	

Products & Tests vs. Models (2)

		Resp.	EM	AVM	CQM	PFM	FS	Comments
Simulators								
FPU Simulator								Developed by CEA/SIG
	Electronics	SAp	1			1		
	Mechanics	CAp	1			1		
DRCU Simulator								
	H/W							
	Station	SO	2	1				
	Elect. Interface	SO	2	1				
	S/W							
	Simulation S/W	SO	V0	V1	V2			
Test Facilities								
EGSE								
	Station	Can.	4					
	Elect. Interface	Can.	4					
Local Test Unit								Developed by CEA/SIG
	Station		2					
	Elect. Interface		2					
Test Facility S/W								
	ODDH Interface Emulation	SIG	1					Local Test Unit
	RTA Common	RAL	1					
	RTA Specific	RAL	1					
	QLA	RAL	1					
	Telecom. Generation Tool	RAL	1					
Tests								
	EMC							
	Thermal Vacuum							
	Vibration							


Focal Plane Unit
(FPU)
Cal P
Source
Cal S
Source
Chopper
FTS
Optics
Baffles
Filters
Structure
Shutter
Cooler
P1
Array
P2
Array
P3
Array
S1
Array
S2
Array
JFET
Optical Bench
Buffer Amplifier Unit (BAU)
Cryostat Wall
Detector Read-out & Control Unit (DRCU)
Warm Interconnect Harness (WIH)
Digital Processing
Unit (DPU)
Signal Processing Unit
(SPU)
SVM


Structure
Optics
Mirrors
Filters
Baffles
Detector Subsystem
Photometer Arrays
Spectrometer Arrays
Cooler
Focal Plane Unit
Chopper
Spectrometer
Calibration Sources
Photometer Calibration Source
Spectrometer Calibration Source
Shutter
JFET Module (TBC)
Buffer Amplifier Unit
Detector Readout and Control Unit
Warm Electronics
Signal Processing Unit
DSP
SPU On Board Software
Power Supply Unit
Digital Processing Unit
On Board Computer
DPU On Board Software

SPIRE Instrument Development Plan

- **Subsystem Qualification and Verification**
  - *Subsystem Qualification*
    - Qualification matrix to be addressed
  - *Subsystem Integration and Testing*
    - Performance testing
    - Environmental Testing
  - *Subsystem Test Facilities*
    - Where, who, how?
- **System-Level Qualification and Verification**
  - *Qualification:*
    - matrix to be addressed
  - *AIV Plan*
  - *Test Facilities*

Subsystem-level Qualification Test Matrix:

	Structure	Optics	FTS Mechanism	Chopper	Detector arrays	Cooler	Filters/grids/dichroics	Calibration Sources	DCRU	SPU	DPU
Vibration:	X	X	X	X	X	X	X	X	X	X	X
Thermal cycle:	X	X	X	X	X	X	X	X			
Vacuum cycle			X	X	X	X	X	X	X	X	X
Lifetime:		P	X	X	X	X	X	X	X	X	X
Soak/cycle:			X	X	X	X		X	X	X	X
Radiation tolerance:			P	P	X	P	X	X	X	X	X
Thermal range:			X	X	X	X	X	X	X	X	X
Thermal stability:		P	X	X	X	X	P	X	X	X	X
Microphonics:		P	X	X	X	X	P	P			
Ionising radiation:					X						
EMI:			X	X	X	P		P	X	X	X
EMC:			X	X	X	P		P	X	X	X

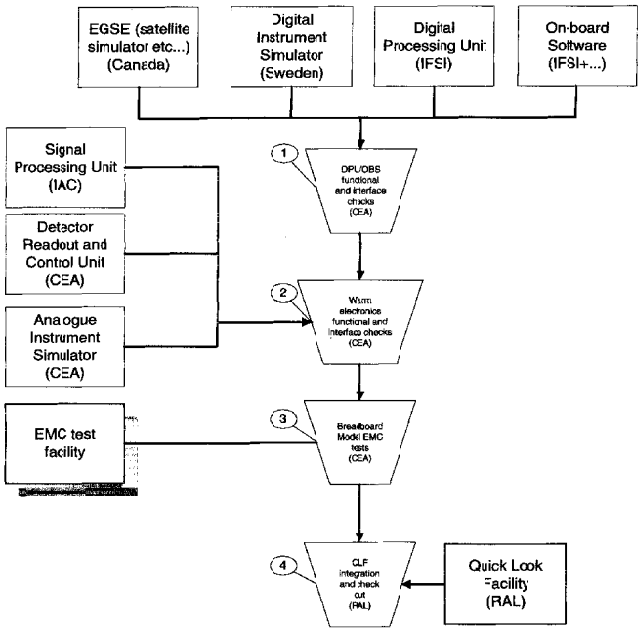
Table 3.1.1: Test matrix for the SPIRE sub-systems qualification programme. Tests marked with an X are mandatory, those marked with a P are possibly required depending on the detailed design of the sub-system and/or the new of novel materials. The requirement to carry out the test programme indicated here has a requirement ID of IRD-SUBS-01

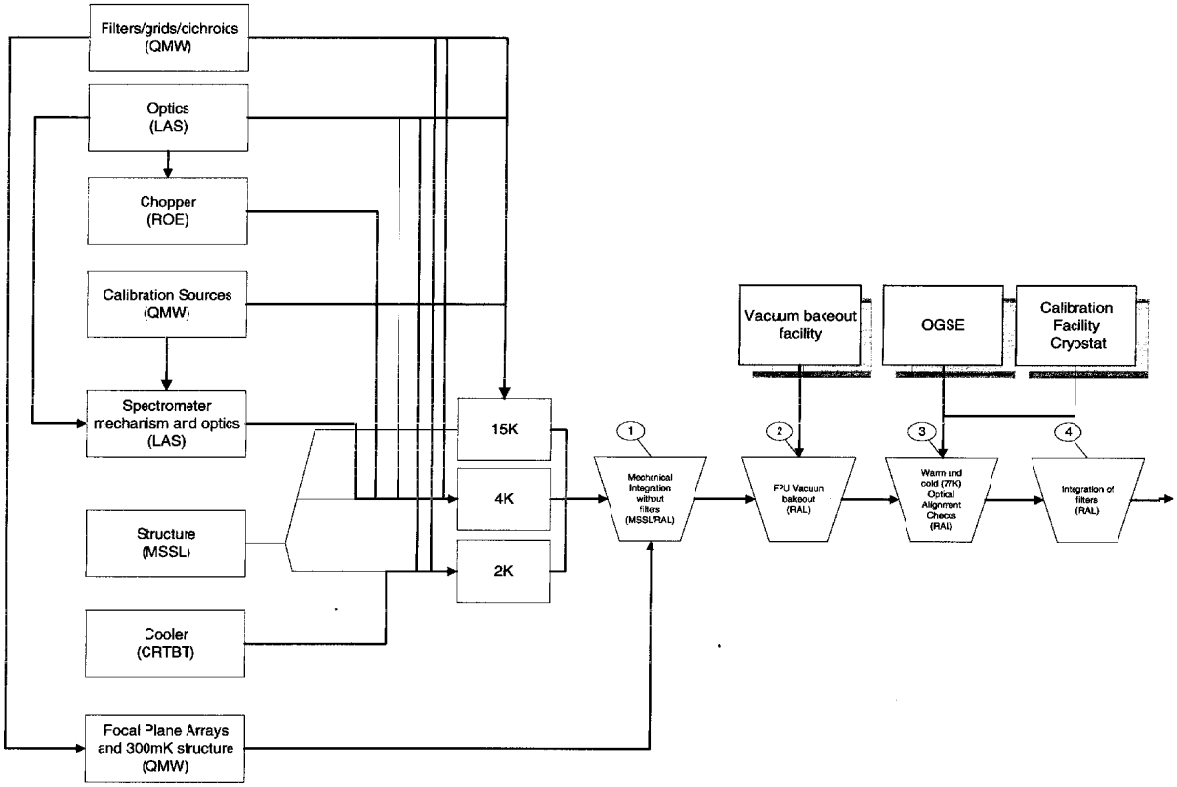
For some sub-systems the qualification and lifetime testing will be more appropriately carried out at component or test item level rather than at the level of the integrated sub-system. At what stage and under what conditions the tests are to be carried out is a matter for detailed consideration by the groups responsible for the sub-systems delivery.

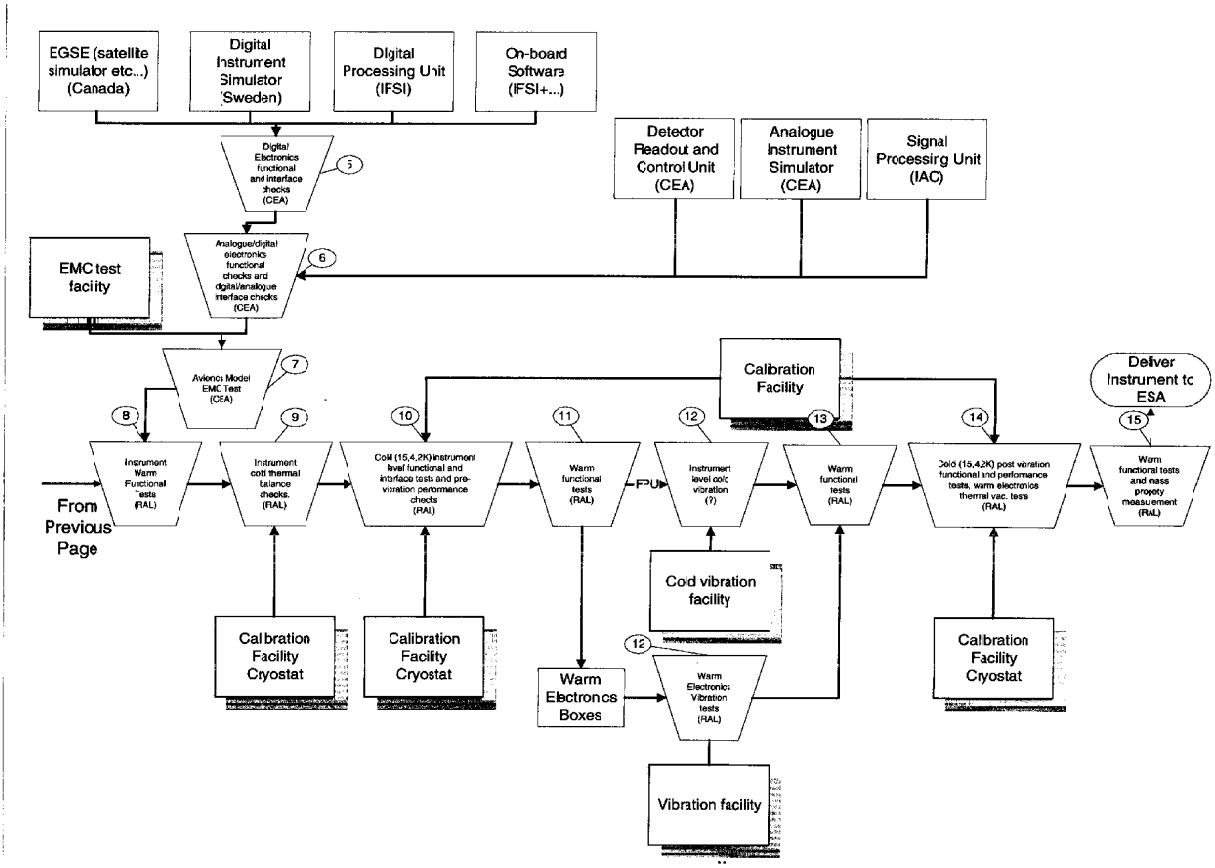
Instrument-level Qualification Test Matrix

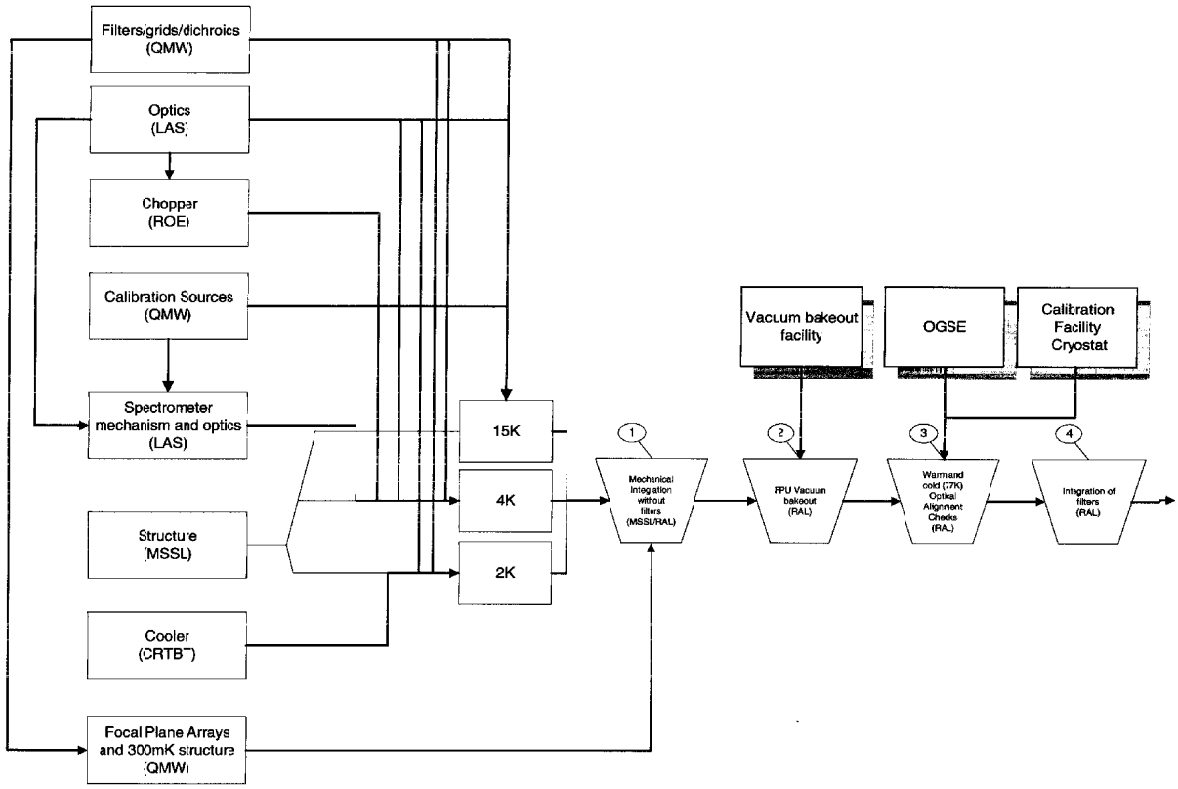
	CQM FPU	CQM DCRU	CQM SPU	CQM DPU	PFM FPU	PFM DCRU	PFM SPU	PFM DPU	FS Focal Plane Unit	FS DCRU	FS SPU	FS DPU
Vibration:	Q	Q	Q	Q	QA	QA	QA	QA	A	A	A	A
Thermal cycle:	Q	Q	Q	Q	QA	QA	QA	QA	A	A	A	A
Vacuum cycle	x	x	x	x	x	x	x	x	x	x	X	x
Thermal range:	x	x	x	x	x	x	x	x	-	-	-	-
EMC (Instrument Level)	x	x	x	x	x	x	x	x	-	-	-	-
EMC (Satellite Level):	-	-	-	-	x	x	x	x	-	-	-	-

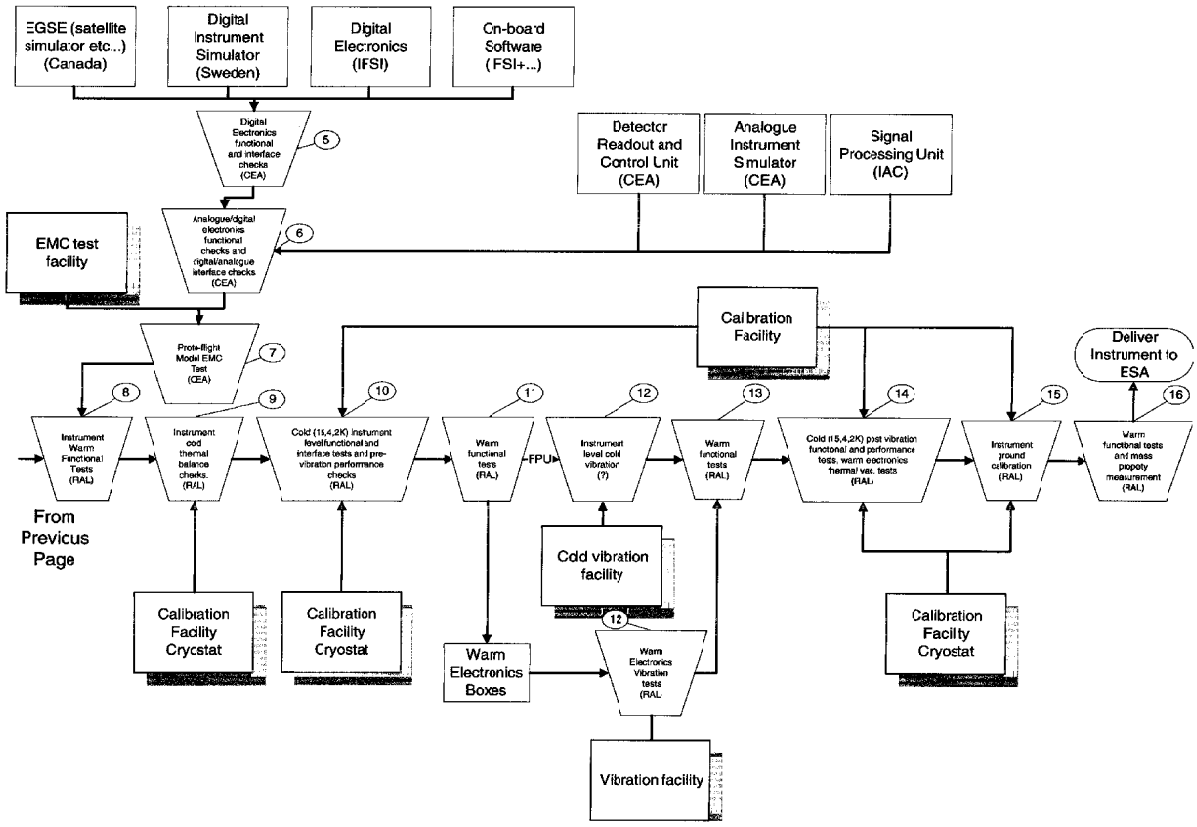
Table 3.2.1: Test matrix for the instrument level testing. Q indicates a test carried out at qualification level for qualification times; QA a test carried out at qualification levels for acceptance test times and A a test carried out at acceptance level for acceptance times. An x indicates that this test is carried out and is a characterisation type test or the level is irrelevant. A dash indicates that no test will be done on this model/unit. The requirement to carry out the test programme indicated here has a requirement ID of IRD-INST-R01


EGSE (satellite simulator etc...) (Canada)
Digital Instrument Simulator (Sweden)
Digital Processing Unit (IFSI)
On-board Software (IFSI+...)
Signal Processing Unit (IAC)
Detector Readout and Control Unit (CEA)
Analogue Instrument Simulator (CEA)
EMC test facility
1
DPU/OBS functional and interface checks (CEA)
2
Warm electronics functional and interface checks (CEA)
3
Breadboard Model EMC tests (CEA)
4
CLF integration and check out (RAL)
Quick Look Facility (RAL)


Filters/grids/cichroics (QMW)
Optics (LAS)
Chopper (ROE)
Calibration Sources (QMW)
Spectrometer mechanism and optics (LAS)
Structure (MSSL)
Cooler (CRTBT)
Focal Plane Arrays and 300mK structure (QMW)
15K
4K
2K
1
Mechanical Integration without filters (MSSL/RAL)
Vacuum bakeout facility
2
FPU Vacuum bakeout (RAL)
OGSE
3
Warm and cold (77K) Optical Alignment Checks (RAL)
Calibration Facility Cryostat
4
Integration of filters (RAL)


EGSE (satellite simulator etc...) (Canada)
Digital Instrument Simulator (Sweden)
Digital Processing Unit (IFSI)
On-board Software (IFSI+...)
Detector Readout and Control Unit (CEA)
Analogue Instrument Simulator (CEA)
Signal Processing Unit (IAC)
Digital Electronics functional and interface checks (CEA)
5
EMC test facility
Analogue/digital electronics functional checks and digital/analogue interface checks (CEA)
6
Avionic Model EMC Test (CEA)
7
Calibration Facility
Deliver Instrument to ESA
8
9
10
11
12
13
14
15
From Previous Page
Instrument Warm Functional Tests (RAL)
Instrument cold thermal balance checks. (RAL)
Cold (15,4,2K) instrument level functional and interface tests and pre-vibration performance checks (RAL)
Warm functional tests (RAL)
FPU
Instrument level cold vibration (?)
Warm functional tests (RAL)
Cold (15,4,2K) post vibration functional and performance tests, warm electronics thermal vac. tests (RAL)
Warm functional tests and mass property measurement (RAL)
Cod vibration facility
Calibration Facility Cryostat
Calibration Facility Cryostat
Warm Electronics Boxes
12
Warm Electronics Vibration tests (RAL)
Calibration Facility Cryostat
Vibration facility


Filters/grids/dichroics (QMW)
Optics (LAS)
Chopper (ROE)
Calibration Sources (QMW)
Spectrometer mechanism and optics (LAS)
Structure (MSSL)
Cooler (CRTB)
Focal Plane Arrays and 300mK structure (QMW)
15K
4K
2K
Vacuum bakeout facility
OGSE
Calibration Facility Cryostat
1
2
3
4
Mechnical Integration without filters (MSSL/RAL)
FPU Vacuum bakeout (RAL)
Warm and cold (77K) Optical Alignment Checks (RAL)
Integration of filters (RAL)


EGSE (satellite simulator etc..) (Canada)
Digital Instrument Simulator (Sweden)
Digital Electronics (IFSI)
On-board Software (FSI+..)
Digital Electronics functional and interface checks (CEA)
5
Detector Readout and Control Unit (CEA)
Analogue Instrument Simulator (CEA)
Signal Processing Unit (IAC)
EMC test facility
Analogue/digital electronics functional checks and digital/analogue interface checks (CEA)
6
Calibration Facility
Deliver Instrument to ESA
Proto-flight Model EMC Test (CEA)
7
8
9
10
11
12
13
14
15
16
Instrument Warm Functional Tests (RAL)
Instrument cod thermal balance checks. (RAL)
Cold (1i,4,2K) instrument levelfunctional and interface tests and pre-vibration performance checks (RAL)
Warm functional tess (RAL)
FPU
Instrument level cold vibration (?)
Warm functional tests (RAL)
Cold (15,4,2K) pst vibration functonal and performance tess, warm eectronics thermal vac. tests (RAL)
Instrument ground calibration (RAL)
Warm functonal tests and mass popoty measurement (RAL)
From Previcus Page
Calibration Facility Cryostat
Calibration Facility Cryostat
Cdd vibration facility
12
Warm Electronics Boxes
Warm Electronics Vibration tests (RAL
Calibration Facilty Cryostat
Vibration facility

SPIRE Instrument Development Plan

- **Status of Subsystem Development Information**
  - *FPU: Nothing apart from*
    - GSFC: addresses most areas for the CQM, only
    - LAS:
      - Optics: OK
      - FTS: doesn't yet address qualification and testing
  - *Warm Electronics: Nothing apart from*
    - IFSI: doesn't yet address qualification and testing