SPIRE Warm Electronics Group Meeting #1.
March 24-25, 1999
CEN Saclay - SAp

Attendees:

IAC : I.Perez
IFSI: R.Cerulli, R.Orfei
LAS : D.Ferrand, D.Pouliquen
SAp : J-L.Auguères, C.Cara, F.Loubère, L.Rodriguez, L.Vigroux
RAL : K.King

Distribution list:

Attendees + C.Cunningham, W.Gear, M.Griffin, B.Swinyard
J.Herreros, H.G.Floren (SO)

1. Main outcomes of the FST meeting (LV).

- The FIRST PM confirms that work is ongoing on telemetry rate issue (aim 200kbps) Confirmation by end of May.
  Action on PIs to argue on the advantage. by Apr. 15.
- Cryo vibration facility. ESA issued specifications. Call for proposal (labs & industry).
- Telescope: Proposal for a segmented telescope (6 sectors mechanically & thermally independents). Baseline 3.5 m telescope.
  Action on PIs to asses this design for their instruments.

2. Managerial issues.

2.1 SPIRE organisation (KK).

- From the management plan (see viewgraphs).

2.2 Schedules(short & long term) (KK).

Overall development schedule and and a more detailed schedule (up to the CDR) were presented (see viewgraphs).

- PDR issue:

  - LR: suggests to call it Internal Review (not involving ESA).
  - LV: we agree that we need a review but not called PDR. See HIFI review outcomes which were very damaging for this project.
  - LV: a real PDR has to take place in mid 2000 anyway.
  - KK: agrees to change the name.

- FTS issue:

  DP:
  - FTS mechanism will be subcontracted (ITT to be issued by the end of 1999).
  - Because requirements have to be stated first, no preliminary design can be produced earlier than mid 2000.
  - From ISO experience it took one year for SRON to produce a model.
  - CQM will be late by one year due to the lack of specification (detectors, optics, mechanics,...
  - The CQM readiness review delays the building of the flight model by one year.

- KK, LR:
  - Requirements on FTS should be available by Summer 99 (except mechanical interface).

  JLA: stressed that this problem has to be raised at System level (System team to deal with).

- JLA: Schedule is still based on the ESA baseline which is at the moment still not compatible with funding profiles of funding agencies (e.g. CNES).

- Short term: work to be done to the PDR (Sept. 1999 for the electronics). Objectives and needed inputs have to be clearly stated.

ACTION on KK: to issue a note stating both objectives and and expected inputs for the Sept. 99 PDR.

2.3 Organization of the WE team (JLA)

See viewgraphs.

- Organization: JLA stressed that the RTA/QLA activity should be strongly linked with the WE as RTA/QLA s/w is intended to be used for WE I&T purpose.
- WE meetings: Agreement on periodic WEG meetings (quarterly is the baseline) and specific WE meetings on specific subjects.
- Reporting: Frequency and efficiency of the reports were discussed. KK recognized that the lack of Workplan and Schedule does not help but insisted on the necessity of keeping monthly reporting.
- Participation to CWGs: JLA pointed out that it has to be clear that the CWG do not have to take decisions in lieu of the Instruments and ask to KK as Commonality Steering group member to take care.
- WE documents: KK stressed that IID-A is to be considered as an input document for the WE as well. JLA pointed out that most of the input documents are preliminary (when they are existing) and do not allow to progress in the production of the WE reference document.
- Current issues: problems are acknowledged but solutions need time. JLA stressed that the System Team has no working plan and does not work in fact as a real team. As a consequence, a lot of system issues remains pending.

2.4 Action review (JLA).

See viewgraphs and Action list summary hereafter.

- Responsible have been designated for the action of the WG meetings.

2.5 Status of the institutes.

2.5.1 SAp (JLA).

See viewgraphs.

2.5.2 IFSI (RC).

See viewgraphs.

- DSP is the baseline. The SPARC option has been implicitly rejected.
  - JLA: remarks that no serious and formal comparison has been made so far.
- Arguments based on requirements have to be put forward.
- Mandatory requirements should be stated.
- DPU ITT issue. Requirements to be frozen by June 99.

2.5.3 IAC.

See viewgraphs.

- Definition of a prototype with the industry.
  - JLA: pointed out that SPIRE is not in the loop.
  - JLA: emphasized that IAC has not produced and presented a development plan for agreement (see action on IAC from the SAp/IAC meeting).
  - KK : Insisted on the necessity to get a Development plan at short notice.
  - Critical dates have to be defined.

  LR: Requirements are not stable. Computing options depending on data transmission rate.
  KK: We need assessment on science degradation in case of lower telemetry rate.

ACTION KK to talk with the other project manager about design synchronization of the different groups.

2.5.4 LAS (DP).

- DP raises concern about the PDR preparation at no design will be available by this time (realization by a subcontractor).

2.5.5 SO.

- SO was not represented at this meeting.

ACTION on KK to contact SO to asses the situation.

3. <u>Warm Electronics requirements and constraints</u> (CCa).

3.1 Review of existing requirements and shade areas (missing parameters and requirements).

See viewgraphs.

System reliability.
- L2 orbits: Solar flares are the constraint drivers (proton).

Autonomy issue.
- No automatic reconfiguration can be performed onboard.
- Safety requirements: wrong commanding shall not damage the instrument.
- LV: power supply measurement should be taken into consideration.

Glitches rejection.
- LV: the best solution is to send co-added image with a flag telling were glitches have to be found (instead of putting the pixel value to 0).

TRANSPARENT mode:
- Could be considered as an observing mode.

Transmission rate:
- JLA: Dead times have to be taken into consideration (i.e. the instrument does not perform acquisition all the time).
- KK: Could be as high as 50% if we take the S/C moving into consideration.

Instrument Performance:

- Dynamic range: ADC converter and oversampling combination.
  14 bits for the Photometer & 16 bits for the Spectrometer (not needed if compensation).
- Number of pixel.
  Decision to be taken at the System level (next System meeting?).

List of functions.

- Table to be commented.

JLA: Proposal to use a formal method to functionally describe the system. Status diagrams could be a simple way.

3.2 WE Budgets.

See viewgraphs.

3.3 S/C Interfaces.

- H/W interface chip exists (see viewgraphs). It use DMA access.
- Very little is known about the high level protocol.

3.4 Commonality issues.

- All is covered by the IORD.

4. Development plan.

4.1 SPIRE development plan (KK).

- Only preliminary draft is currently available.
- Model definitions are not yet stable and are not consisten with the IID-B.
- A detailed schedule is still to be produced.

4.2 WE development plan (JLA).

Discussions were mainly based on the models and the number and characteristics of the subsystems.

It has been decided that the Bread Board Model will be renamed as Engineering Model (EM)

JLA presented a table (attached to these minutes) which has been discussed and completed as far as possible during the discussions.

EM (former BBM):

- IFSI will build (through industry) 2 Avionics models.
  One could be used for the BBM.
  Is 2 boards enough?

AVM:

- Redundancy issue unclear (redundance interface tests with the s/c?).
- DRCU simulator needed and/or FPU simulators era needed..

ACTION on IAC/JH to check the Model table figures for the SPU.

ACTION on the System team to perform a risk analysis.

5. WE Quality Assurance (FL).

See Viewgraphs.

- Francoise Loubere is the WE PA responsible.
- FL stressed that no QA activity has been started at SPIRE level. As a consequence, the WE QA Plan cannot take into account SPIRE QA requirements.
- It is expected that the SPIRE PA manager organise and monitor the subsystem PA activities.

ACTION on KK to boost the SPIRE QA activity.

+ Actions from the list presented by FL and included in the meeting's action list hereafter.

- IFSI (RO) Contract will be placed in the industry. Contracts will include QA requirements. JLA: Industry QA practices are to be monitored IFSI QA plan shall reflect this.
- RO: Procedures in fact exist for the electronics. JLA stressed that it has to be checked that procedures cover the QA requirements.
- DF: do exist special reliability, availability requirements?

6. Warm Electronics design.

6.1 Overall architecture.

SPU/DPU vs. DPU alone discussion.

Discussions were based on the note issued by SAp and inputs made by IFSI.

LV:
- stressed that with respect to the one CPU solution (DPU alone), we are expecting global gains in term of cost, reliability and risk.
- recall that the past experiences show that nothing remains as simple as foreseen.
- necessity to have open discussions to look at the technical basis.

KK:
- emphasized that we should demonstrate why the current baseline is inadequate.

LV:
- decision has to be taken at high level (system or steering groups).

RC:
- pointed out that given the necessity to submit an ITT by the end of the year, we need a close deadline.

It has been agreed that the single CPU solution (DPU alone) is feasible with respect to the pure technical aspects.

LV depicted the 3 possible cases:

2 CPUs:

- Baseline: IFSI provide the DPU, IAC the SPU and the SPU memory boards.

1 CPU:

- DPU Based: IFSI provide the DPU and IAC provide the memory board.
- SPU Based: IAC provide both the CPU and the memory boards.

It has been agreed that:

- the note issued by JLA will be completed and circulated.

ACTION on JLA to complete and circulate the note on DPU/SPU vs. DPU options.

- this note will be discussed at the next Science meeting in Marseille (Apr. 27, 1999).

6.2 Detector technology impact.

See viewgraphs.

Impact of the 3 options (CEA, JPL, GFSC) were presented and discussed.

6.3 Redundancy issues.

Overall redundancy scheme and options were presented and discussed (See viewgraphs).

JLA stressed that to keep the electronics design consistent, the redundancy issue has to be addressed at Instrument system level first, then at the WE system level.

ACTION on the System Team: to produce redundancy requirements at system level.

6.4 Power supply and grounding scheme.

A distributed single points scheme has been presented (see viewgraphs).

6.5 Part list.

An action is pending on FIRST/Planck Instruments teams to provide their part list (see CWG #2 action list).

7. Subsystem development.

7.1 DPU

7.1.1 h/w.

- See IFSI viewgraphs.

The choice of the type of processor has been discussed. It is agreed that the DSP is the baseline although certainly not the best choice compared to the SPARC to run Real Time multitask s/w.

The DPU shall comply with a set of SPIRE requirements whatever their compatibility with common requirements. These requirements are mainly dealing with:

- the number and performance of DMA channels.
- RAM addressing capability (depending on the options chosen).
- watchdog.
- real-time clock.
- ...

Given the subcontract consideration stated above by IFSI, these requirements have to be stated quickly. They are however linked to the system design of the instrument and of the warm electronics.

7.1.2 s/w functionality.

- See IFSI viewgraphs.

- Real-Time system:

  Virtuoso is undergoing an evaluation process from the instrument teams (including IFSI).

  DF pointed out that Virtuoso, planned to be used by Corot, has finally been rejected (contact Remi Belanger at Meudon). The main reason was the poor efficiency of the available development s/w (compiler).

  IFSI envisage the possibility of the development of a home made Real Time kernel.

7.2 SPU & Memory boards.

No additional information provided by IAC at this meeting on both h/w & s/w aspects.

Like for the DPU, requirements have to be stated prior to any development. The requirement are depending on the options chosen as well.

7.3 DRCU.

- Block diagram show by CC (see viewgraphs).
- System issue: should h/k parameter be merged with science data on demand (rate acquisition issue) for testing and investigation purpose.

7.4 BAU.

- Detector type dependent.
- Prototyping ongoing at SAp (CEA option).

7.5 Harness.

See interconnection diagram viewgraphs.

7.6 FTS control electronics.

- Nothing presented by LAS.

7.7 Chopper electronics.

- Chopper situation is still unclear.
- No inputs were presented at the meeting.

8. Test facilities

8.1 ESGE (h/w & s/w (RTA)).

- The EGSE is needed locally (at IFSI and at SAp) for I&T purpose.
- It shall interface directly to the DPU without having to use FINDAS.
- The EGSE shall run basic telecommanding and display s/w.
- Generation of telecommand sequence (e.g. related to the monitoring of an instrument mode on an observation) have to be available.
- The EGSE shall run RTA/QLA s/w or have the suitable interface with an RTA/QLA station.

8.2 Local test unit.

- The Local test unit is needed for test & integration of the WE.
- Depending on the WE architecture (one or two CPUs) the Local test unit could be interfaced with the DRCU and the SPU.
- It will be developed by the CEA and is not intended to be delivered.
- It will likely consist of a PC and suitable h/w interfaces.
- The s/w will have a command generation part and a monitoring, recording and display part. This last part could encompass the RTA/QLA software.

8.3 Simulators (digital & analog).

8.3.1 Digital simulator.

- This simulator shall interface with the DPU (or SPU) and simulate the DRCU.
- It is needed for I&T purpose and could be delivered as part of the AVM to ESA (see model definition issues above)
- This simulator should be provided by SO.

8.3.2 Analog simulator.

- It shall simulate the FPU (behind and/or before the BAU).
- It is needed for I&T purpose and End to End tests.
- It will be built and provided by the CEA.

9. Integration and Test.

9.1 SPIRE AIV.

- No additional information than those included in the SPIRE IDP.

9.2 WE AIV.

- Draft plan to be produced.

10. Preparation of the electronics PDR.

See section 2.2.

Action List:

- WEG meeting #1 - Saclay - March 24-25, 1999

Action 1	KK		Open	to issue a note stating both objectives and expected inputs
Action 2	KK		Open	to talk with the other project manager about design synchronization of the different groups.
Action 3	KK		Open	to contact SO to asses the situation.
Action 4	IAC/JH		Open	to check the Model table figures for the SPU.
Action 5	System team		Open	to perform a risk analysis.
Action 6	KK		Open	to boost the SPIRE QA activity.
Action 7	RAL/GD	asap	Open	Issue the SPIRE Quality Requirements
Action 8	KK	asap	Open	Provide the list of documents to be produced for the PDR
Action 9	SAp/FL	04/99	Open	Produce the first issue of the Warm Electronics Product Assurance Plan
Action 10	SAp/FL	05/99	Open	Produce the first issue of the Warm Electronics Quality requirements.
Action 11	WE Inst.	asap	Open	Appoint a Quality Manager (or correspondent)
Action 11	WE Inst.	06/99	Open	to produce their Product Assurance Plans.
Action 12	JLA		Open	to complete and circulate the note on DPU/SPU vs. DPU options.
Action 13	System Team		Open	to produce redundancy requirements at system level.

WEG Actions from previous meetings

- SAp/IAC meeting - IAC - Nov. 16, 1998

Action 1	IAC/JH		Open	Draft an SPU Development Plan

- Warm electronics & S/W working group splinter meeting (SPIRE Consortium Meeting - RAL - Dec. 1-2, 1998)

Action 2	BMS	20/01/99	Open	To respond the essential input request list.
Action 3	KJK	15/12/99	Open	To provide a Development Plan containing AIV information as well..
Action 4	SAP/LR	15/01/99	Open	To draft a skeleton of the electronics specifications with the electronics requirements identified so far.

- SAp/IFSI meeting - IFSI - Feb. 16, 1999

Action 1	KJK	asap	Open	To provide asap a reasonably stable version of the SPIRE development plan (including schedule and a flow diagram).
Action 2	IFSI & SAp	15/03/99	Open	Comment the preliminary draft of the SPIRE Development Plan.

WEG related CWG Actions

- CWG #4 - Feb. 10, 1999

Action 3	JLA	20/05/99	Open	SPIRE to confirm allocation of responsibilities for SPU h/w & s/w implementation.
Action 5	IRC (*)	06/05/99	Open	Generate and Co-ordinate "requirements" on instrument commanding & verification.
Action 7	RC/JLA	06/05/99	Open	Define OBSW related milestones and activities till end 99.
Action 8	KK	06/05/99	Open	Provide comments to Appendix 1 of Mission Operation Scenario.

(*) Draft to be sent to WEG, then to the System team.

- CWG #3 - Feb. 3, 1999

Action 3	KK	19/05/99	Open	Provide plans for ILTs, indicating required deliveries (S/C simulator, CCE,...)
Action 8	KK	30/04/99	Open	Comment on PACS RTA requirements used for SCOS testing.
Action 9	KK	05/03/99	Open	To supply estimates of manpower available for RTA related activities.

- CWG #1 #2 - March 3, 1999

Action 1	RO	25/05/99	Open	Submit list of needed common parts.

Products & Tests vs. Models (1)

		Resp.	EM	AVM	CQM	PFM	FS	Comments
WE UNITs								
DPU								
	Electronics							
	CPU Board	IFSI	1	1	2	2	(2/3)	FS shared with other Inst.
	Memory	IFSI	1	1	2	2	(2/3)	
	Power Supply	IFSI	1	1	2	2	(2/3)	
	Component Grade		Std	Std	Mil	Qual	Qual	
	Mechanics							
	DPU Box	IFSI	1	1	1	1	(1/2)	FS shared with other Inst.
	Connectors	IFSI	X	X	X	X	X	
	S/W							
	LL s/w	IFSI	V0	V1	V1	V flight	V flight	
	HL s/w	IFSI	V0	V1	V1	V flight	V flight	
SPU								
	H/W							
	CPU Board	IAC	1	1	2	2	1	
	Memory	IAC	xMo	xMo	2*(xMo)	2*(xMo)	xMo	
	Power Supply	IAC	1	1	1	1	1	
	Component Grade		Std	Mil	Mil	Qual	Qual	
	Mechanics							
	SPU Box	IAC	1?	1	1	1	(1/2)	FS shared with other Inst.
	Connectors	IAC	X	X	X	X	X	
	S/W							
	LL s/w	IAC	V0?	V1?	V1?	V flight	V flight	
	HL s/w	SAp	V0?	V1?	V1?	V flight	V flight	
DRCU								
	Electronics							
	Detector Readout	SAp	1	-	1	1	1	
	FTS Control	LAS	1	-	2	2	1?	
	Cryo Control	SAp	1	-	2	2	1?	
	Chopper Control	SAp	1	-	2	2	1?	
	Calib. Source Control	SAp	1	-	2	2	1?	
	H/K readout	SAp	1	-	2	2	1?	
	Component Grade		Std	-	Mil	Qual	Qual	
	Mechanics							
	DRCU Box	SAp	1	-	1	1	1	
	Connectors	SAp	X	X	X	X	X	
BAU								
	Electronics							
	Buffers	SAp	1		1	1	1	
	Temp. Regulation	SAp	1		1	1	1	
	Component Grade		Std		Mil	Qual	Qual	
	Mechanics							
	BAU Box	SAp	1	2	2	2	1	
	Connectors	SAp	X	X	X	X	X	
Harness								
	DPU to SPU	SAp	1	1	2	2	1	
	SPU to DRCU	SAp	1	1	2	2	1	
	DRCU to BAU	SAp	1	-	2	2	1	

Products & Tests vs. Models (2)

		Resp.	EM	AVM	CQM	PFM	FS	Comments
Simulators								
FPU Simulator								Developed by CEA/SIG
	Electronics	SAp	1			1		
	Mechanics	SAp	1			1		
DRCU Simulator								
	H/W							
	Station	SO	2	1				
	Elect. Interface	SO	2	1				
	S/W							
	Simulation S/W	SO	2	1				
Test Facilities								
EGSE								
	Station	Can.	4					
	Elect. Interface	Can.	4					
Local Test Unit								Developed by CEA/SIG
	Station		2					
	Elect. Interface		2					
Test Facility S/W								
	OBDH Interface Emulation	SIG	1					Local Test Unit
	RTA Common	RAL	1					
	RTA Specific	RAL	1					
	QLA	RAL	1					
	Telecom. Generation Tool	RAL	1					
Tests								
	EMC							
	Thermal Vacuum							
	Vibration							