# May 6th Agenda

| | | | |
|---|---|---|---|
| 9.30 | Review of the agenda | JLA | 10' |
| 9.40 | Managerial issues | | |
| | - Action review | JLA | 15' |
| | - SPIRE Project info | KK | 15' |
| | - Institute Progress report: | | |
| | . IAC | JH | 5' |
| | . IFSI | RC | 5' |
| | . LAS | DP | 5' |
| | . SAp | JLA | 5' |
| | . SO (full status) | HGF | 10' |
| 10.40 | SPIRE System status | LR/BS | 20' |
| 11.00 | WE Quality Assurance. | | |
| | - SPIRE QA Plan | KK/GD | 10' |
| | - WE QA progress report | FL(JLA) | 5' |
| 11.15 | Coffee break | | |
| 11.30 | WE system issues. | | |
| | - Review and discussion about the existing and missing WE requirements | JLA/CC | 90' |
| 13.00 | Lunch | | |
| 14.00 | WE functional analysis. | CC | 90' |
| | - Discussions on the Instrument status diagram. | | |
| | - WE functionality to be fulfilled to meet the WE requirements. | | |
| 16.20 | Short term planning (building and discussions) | JLA/KK | 20' |
| 16.40 | DPU/SPU option status | | |
| | - Outcomes of the last Steering Group meeting | KK | 10' |
| | - Other inputs since the last meeting: | | |
| | . IFSI and IAC comments. | RC | 10' |
| | . MMS CPU board: info collected so far, possible impact on the SPIRE WE. | CC | 15' |
| 17.15 | AOBs | | |
| 17.30 | End of meeting. | | |

## Pending Actions

- WEG meeting #1 - Saclay - March 24-25, 1999

| | | | | |
|---|---|---|---|---|
| Action 1 | KK | | Open | to issue a note stating both objectives and expected inputs |
| Action 2 | KK | | Open | to talk with the other project manager about design synchronization of the different groups. |
| Action 3 | KK | | Open | to contact SO to asses the situation. |
| Action 4 | IAC/JH | | Open | to check the Model table figures for the SPU. |
| Action 5 | System team | | Open | to perform a risk analysis. |
| Action 6 | KK | | Open | to boost the SPIRE QA activity. |
| Action 7 | RAL/GD | asap | Open | Issue the SPIRE Quality Requirements |
| Action 8 | KK | asap | Open | Provide the list of documents to be produced for the PDR |
| Action 9 | SAp/FL | 04/99 | Open | Produce the first issue of the Warm Electronics Product Assurance Plan |
| Action 10 | SAp/FL | 05/99 | Open | Produce the first issue of the Warm Electronics Quality requirements. |
| Action 11 | WE Inst. | asap | Open | Appoint a Quality Manager (or correspondent) |
| Action 11 | WE Inst. | 06/99 | Open | to produce their Product Assurance Plans. |
| Action 12 | JLA | | Open | to complete and circulate the note on DPU/SPU vs. DPU options. |
| Action 13 | System Team | | Open | to produce redundancy requirements at system level. |

- SAp/IAC meeting - IAC - Nov. 16, 1998

| | | | | |
|---|---|---|---|---|
| Action 1 | IAC/JH | | Open | Draft an SPU Development Plan |

- Warm electronics & S/W working group splinter meeting (SPIRE Consortium Meeting - RAL - Dec. 1-2, 1998)

| | | | | |
|---|---|---|---|---|
| Action 2 | BMS | 20/01/99 | Open | To respond the essential input request list. |
| Action 3 | KJK | 15/12/99 | Open | To provide a Development Plan containing AIV information as well.. |
| Action 4 | SAP/LR | 15/01/99 | Open | To draft a skeleton of the electronics specifications with the electronics requirements identified so far. |

- SAp/IFSI meeting - IFSI - Feb. 16, 1999

| | | | | |
|---|---|---|---|---|
| Action 1 | KJK | asap | Open | To provide asap a reasonably stable version of the SPIRE development plan (including schedule and a flow diagram). |
| Action 2 | IFSI & SAp | 15/03/99 | Open | Comment the preliminary draft of the SPIRE Development Plan. |

## WEG related CWG Actions

- **CWG #4 - Feb. 10, 1999**

| | | | | |
|---|---|---|---|---|
| Action 3 | JLA | 20/05/99 | Open | SPIRE to confirm allocation of responsibilities for SPU h/w & s/w implementation. |
| Action 5 | IRC (*) | 06/05/99 | Open | Generate and Co-ordinate "requirements" on instrument commanding & verification. |
| Action 7 | RC/JLA | 06/05/99 | Open | Define OBSW related milestones and activities till end 99. |
| Action 8 | KK | 06/05/99 | Open | Provide comments to Appendix 1 of Mission Operation Scenario. |

**(*) Draft to be sent to WEG, then to the System team.**

- **CWG #3 - Feb. 3, 1999**

| | | | | |
|---|---|---|---|---|
| Action 3 | KK | 19/05/99 | Open | Provide plans for ILTs, indicating required deliveries (S/C simulator, CCE,...) |
| Action 8 | KK | 30/04/99 | Open | Comment on PACS RTA requirements used for SCOS testing. |
| Action 9 | KK | 05/03/99 | Open | To supply estimates of manpower available for RTA related activities. |

- **CWG #1 #2 - March 3, 1999**

| | | | | |
|---|---|---|---|---|
| Action 1 | RO | 25/05/99 | Open | Submit list of needed common parts. |

# Meetings

7-8 April : Focal Plane commonality meeting

20-21 April : FINOAS Prototype presentation and demo

26 April : Science team meeting (+ steering committee)

6 May : W.E. meeting

18-20 May : System Team meeting - technical decision on SPU/OPU

Detector meeting - run through of inputs for PDR

CWG (RTA, Operations, FINOAS) meetings

End May : Steering Committee - Decision on SPU/OPU

11 June : FIRST AOCS to Instrument I/F meeting

15 June : CWG (Compacts) meeting

22 June : ESA S/C Systems meeting

5-7 July : FIRST Ground Segment meeting

7-9 July : PDR (Phase 1)

~ 27-30 Sept : PDR (Phase 2)

(TBC) Oct : Instrument Science Verification Review

# SPIRE SCHEDULE

x No change (unless someone knows different!)

End Apr : Development Plan inputs due

End May : Development Plan delivered to ESA

End June : PDR (Phase 1) inputs due

7-9 July : PDR (Phase 1)

~ 27-30 Sept : PDR (Phase 2) ] SPIRE Instrument Science Verification Review

oct? ←

Sept - Dec : Detector Evaluation

Jan : Detector Selection

Feb : Delta PDR

## STATUS

* Development Plan inputs from only 1 group
  THIS MUST BE DONE!

* No comments on Instrument Requirements Document
  - This is not a project responsibility - we are a team

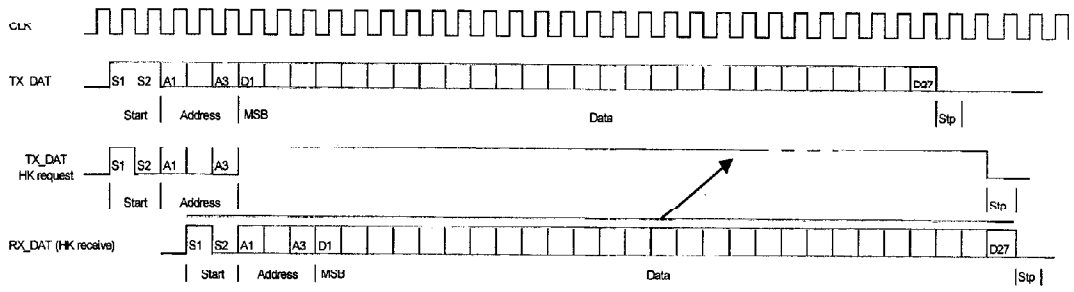
x No inputs to Qualification Plan.
  - needed for PDR (→ IOP)

# IFSI status report

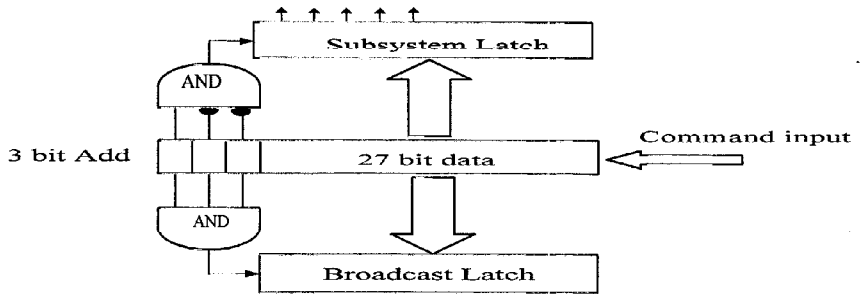
- Upgraded ITT baseline document.
- New meeting with one candidate firm.
- Ready to issue the ITT when SPIRE architecture is decided.
- We have now a good agreement about S/S I/F of HIFI:
  The low speed serial bus will be used also for syncronization (resolution <= 10 us)
  High speed bus signals (clock and gate) are originated by S/S.

# Low speed serial I/F bus

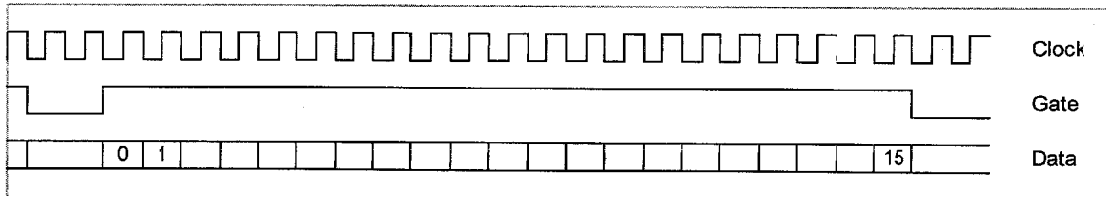
All data transactions with the addressed subsystem (addr. In TX_DAT), are initiated by DPU.
ICU will send data to all subsystems using one serial data line TX_DAT and can send both commands and HK requests via this line.
Subsystems will send responses via RX_DAT line.
A **command** is made of 2 start bit, followed by 30 bit divided in address and data and 1 stop bit. For HIFI we suggest 3 address bit and 27data bit as shown in figure.
**HK request** is made of 2 start bit and the address bit. After transmission of these bit, the TX_DAT line shall stay high until the corresponding HK response has been received. Then 1 stop bit will follow.
A **HK response** shall consist of 2 start bit, 30 address and data bit and 1 stop bit.
The figure shows the proposed HW protocol. Clock rate ~ 100KHz




The 3 address lines allow interfacing with 8 different subsystems each with a different formatting of the data bits. One address (i.e. the addr – 7) can be reserved as a broadcast command, with its own formatting of the data field, which carries information "interesting" for all subsystems. The data field of the broadcast command, if necessary, can be further divided in order to address only part of the subsystems to perform a "partial" broadcast command.
Each subsystem should capture at least the serial commands with its own address plus the broadcast command.
In the next figure it is shown the block diagram of the serial command decoding for subsystem at address 4



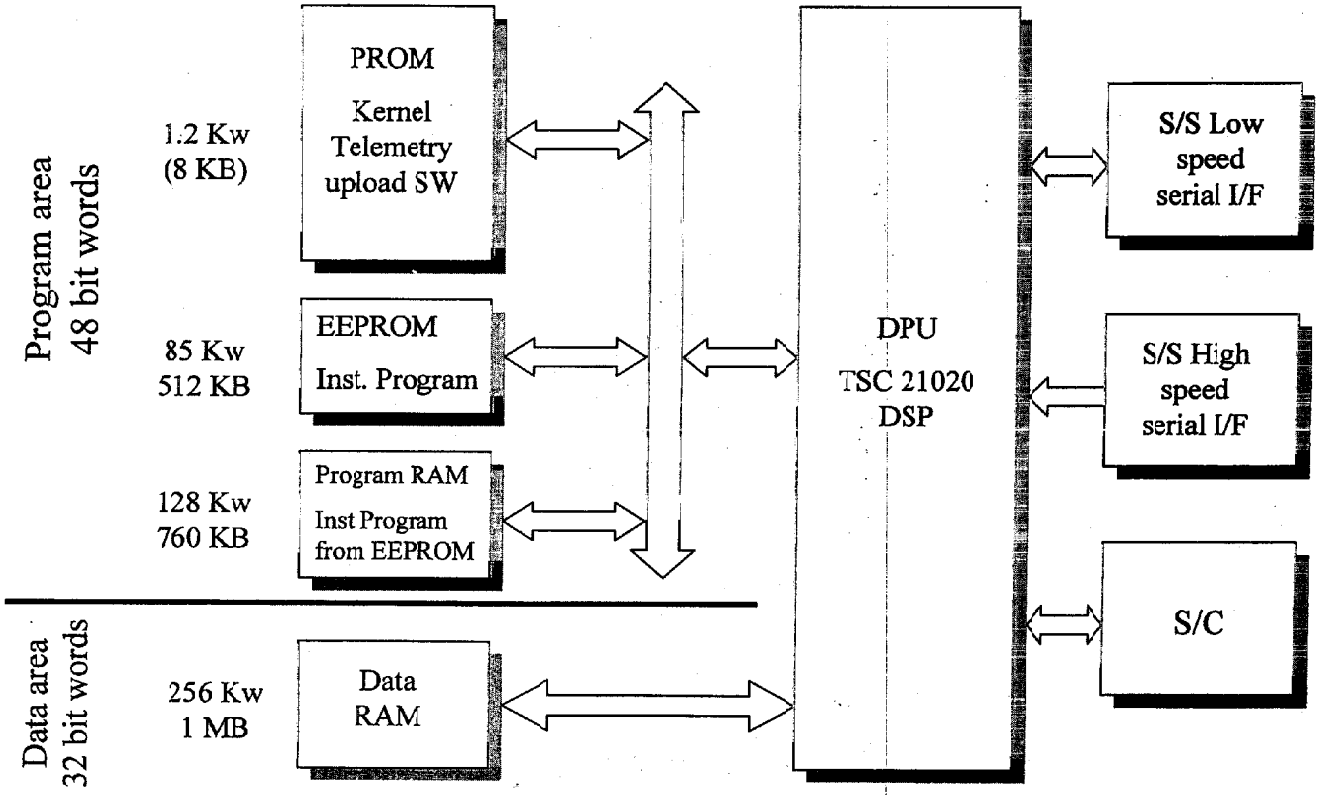
# High speed I/F




- For HIFI we agreed to receive clock, gate (and data) from S/S (clock speed ~ 2MHz).

- For PACS it is very likely that the fast I/F will be based on IEEE Std 1355-1995 (SMCS 332) Synchronous serial high speed link (**196** pin chip).
- We expect a decision on SPIRE DPU-S/S I/F to be taken in a short time.

# Memory organisation



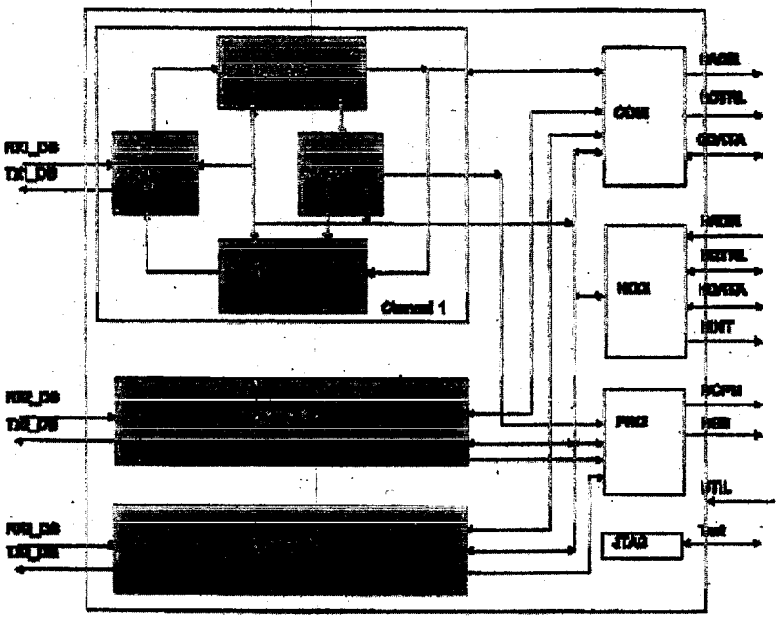

Saclay 6.7.99 ~~Roma 22-23/4/99~~

**Scalable and flexible high performante Serial Communication Controller SMCS 332**

- Three IEEE Std 1355-1995 links (DS-LinkTM): full duplex, up to **200 Mbit/s** (in each direction) point-to-point links
- High-level packet oriented data transfer
- Autonomous command execution
- Fault tolerance features

**Main features:**

- **three** IEEE 1355 serial communication links
- 0 to 200 MBit/s transfer rate per link
- link disconnect detection and parity check at token level
- checksum generation / check at packet level
- available in various quality grades from Temic/MHS in a **196 pin CQFP package,** including, radiation tolerant versions (**50 Krad**, improved SEU performance)
- Interrupt capability for host CPU




Supported by **Virtuoso** Programming System (MP & Synchro, from Eonic Systems) with development and run time tools for a range of multi-processors applications

Saclay 6.5.99 ~~Roma 22-23/4/99~~

| PA ACTIONS PROGRESS | WHO | WHEN |
|---|---|---|
| SPIRE Quality requirements issue (trough PA Plan or specification)<br><br>*Contact has been established with Geoff Douglas on 26/03/99 (by phone). The main points are :*<br>- *requirements expressed at system level in the document ref :SPIRE Product assurance plan, draft 1, 5 Feb 98. No additional requirements should be expressed.*<br>- *CEA in house quality system should be suitable, as used on other projects*<br>- *No further PA action planned for the moment at system level* | RAL | ASAP |
| List of documents to be produced for PDR | RAL | ASAP |
| | | |
| WE PA plan production<br><br>*In progress – some parts still to be written :*<br>*Some PA tasks to be held at CEA level depend of WE architecture choice. Therefore PA plan has been delayed, and first draft will be produced only when architecture choice is made.* | CEA | TBD |
| WE sub system Q requirements<br><br>*In progress in parallel with PA plan*<br>*Production of those requirements will be delayed till decisions on WE architecture are made.* | CEA | TBD |
| | | |
| WE sub systems Quality manager designation | institute | ASAP |
| PA plan production<br>*Depends on production of PA requirements by SAp* | institute | TBD |

# Instrument Functional Requirements.

**High level Requirements.**

| N° | Requirements | Source |
|---|---|---|
| **1.1** | **Shall be able to handle the switched off Mode.** | |
| | | |
| **1.2** | **Shall be able to handle the switched on (idle) mode.** | |
| | | |
| **1.3** | **Shall be able to handle all technological Modes.** | |
| 1.3.1 | Shall be able to handle the **Standby** Mode. | |
| 1.3.2 | Shall be able to handle the **Real time commanding** Mode. | |
| 1.3.3 | Shall be able to handle the **Commissioning/calibration** Mode. | |
| 1.3.4 | Shall be able to handle the **Cryo-cooler** regeneration Mode. | |
| **1.4** | **Shall be able to handle all observing Modes.** | IID-B |
| 1.4.1 | All the Observing modes shall be handled by the means of predefined or up-loaded Procedure Commands eventually combined with Function Commands, Device commands or the individual setting of s/w parameters. | |
| 1.4.2 | It shall be possible to handle Degraded Observing modes by using any combination of the Tele-command capabilities. | |
| **1.5** | **Shall provide facility to control all the devices of the instrument.** | |
| 1.5.1 | Shall provide facility to command individually all devices in the instrument. | OIRD-TC-6 |
| 1.5.2 | The result of any command on any Instrument device shall be verifiable. | |
| 1.5.3 | It shall be possible to get the status of any Instrument device at any time. | |

## Instrument Functional Requirements (cont.).

**Low level requirements.**

| N° | Requirements | Source |
|---|---|---|
| **1.6** | **Shall be able to handle Tele-commands.** | |
| 1.6.1 | Shall perform Tele-command **Verification.** | |
| 1.6.1.1 | Shall **check** the Tele-commands for: correct APID, known service, correct checksum. | OIRD-TCV-2 |
| 1.6.1.2 | Shall generate Tele-command **Acceptance Report** | OIRD-TCV-1& 2 |
| 1.6.2 | Shall be able to **execute** individual Tele-commands | |
| 1.6.2.1 | Shall be able to execute **Immediate** Tele-command. | |
| 1.6.2.2 | Shall be able to execute **Time-tagged** Tele-commands | |
| 1.6.2.3 | Shall be able to execute **Standard** Tele-commands (executed asap) | |
| 1.6.3 | Shall be able to monitor Tele-command **execution progress**. | |
| 1.6.4 | Tele-command **execution** (and or) **progress** shall be echoed in the TM data packets. | |
| **1.7** | **Shall handle Device Commands** | **IRD** |
| 1.7.1 | It shall be possible to pack more than one Device Command into a single tele-command packet in order to carry out a specific onboard function. | OIRD-DVC-2 |
| 1.7.2 | Execution correctness of any Device Commands shall be verified on board. | OIRD-DVC-2 |
| **1.8** | **Shall handle Function Commands** | **IRD** |
| 1.8.1 | Provision shall be implemented to Add, Replace or Delete Functions Commands. | |
| 1.8.2 | A Function Command tele-command packet shall contain at most one Function Command and its parameters. | |
| 1.8.3 | Execution correctness of any Function Commands shall be verified on board. | |
| **1.9** | **Shall handle Procedure Commands** | **IRD** |
| 1.9.1 | Provision shall be implemented to Add, Replace or Delete Procedure Commands. | |
| 1.9.2 | Shall be able to execute and monitor Procedure Commands. | |
| 1.9.3 | A Procedure Command tele-command packet shall contain at most one Function Command and its parameters. | |
| 1.9.4 | Execution correctness of any Function Commands shall be verified on board. | |
| 1.9.5 | The progress of the execution of Procedure Commands shall be verifiable. | |

Instrument Functional Requirements (cont.).

| | | |
|---|---|---|
| **1.10** | **Shall be able to generate TM data packet** | **IRD** |
| 1.10.1 | Shall generate **Standard** science TM data packet corresponding to each observing modes. | |
| 1.10.2 | Shall generate **Diagnostic** science TM data packet corresponding to each observing modes. | |
| 1.10.2.1 | It shall be possible to define up to 8 (TBC) Diagnostic Data packets. | |
| 1.10.2.2 | The transmission rate of Diagnostic Data packets shall be selectable by command between 0.1 to 1000 times per second.. | |
| 1.10.3 | Shall generate **H/K data packet** in all Instrument modes. | IORD-CTRL-4 |
| 1.10.3.1 | Shall generate **Standard H/K** data packet. | |
| 1.10.3.1.1 | Standard H/K data packet shall be generated at **fixed time interval** (0.1 to 10 time per second (nominally 1 second)). | |
| 1.10.3.1.2 | It shall be possible to generate up to 4 types of standard H/K data packet. | |
| 1.10.3.1.3 | The nominal H/K Telemetry packet shall contain all instrument parameters. | |
| 1.10.3.2 | Shall generate **Diagnostic H/K** data packet. | |
| 1.10.3.2.1 | Diagnostic H/K data packet shall contain up to 16 parameters, sampled at a rate selectable between 1 to 1000 times per second. | |
| 1.10.4 | Shall generate **Event packets**. | |
| 1.10.4.1 | Event packet shall be generated each time as an anomaly is recognised by the instrument. | |
| 1.10.4.2 | Each Event packet shall indicate the anomaly type and the data used to identify it. | |
| 1.10.5 | TM data packet shall include a checksum in the data field | |
| **1.11** | **Shall be able to perform Memory Management service.** | **IRD** |
| 1.11.1 | Shall be able to perform Memory Dump | |
| 1.11.2 | Shall be able to perform Memory Up loading | |
| **1.12** | **Shall be able to provide Task Management facility.** | **IRD** |
| 1.12.1 | Provision shall be implemented to Add, Replace or Delete S/W Tasks. | |
| 1.12.2 | It shall be possible to monitor the execution of any S/W task. | |
| 1.12.3 | It shall be possible to reset the whole S/W system. | |
| 1.12.4 | It shall be possible to activate or de activate any S/W task. | |
| 1.12.5 | It shall be possible to mask or de-mask any interrupt level | |
| **1.13** | **Shall be able to handle Time Management & Reporting.** | **IRD** |
| | | |

Functional Requirements from Subsystems.

| N° | Requirements | Source |
|---|---|---|
| 2.1 | Shall be able to perform the detector readout. | |
| 2.3.1.1 | Shall be able to perform the Photometer detector readout. | |
| 2.3.1.2 | Shall be able to perform the Spectrometer detector readout. | |
| 2.2 | Shall be able to monitor the FTS mirror moving. | |
| 2.3 | Shall be able to monitor the Chopper. | |
| 2.4 | Shall be able to monitor the Calibration sources. | |
| 2.5 | Shall be able to monitor the Cryo-cooler system. | |
| 2.6 | Shall be able to monitor the Shutter. | |

S/C Interface requirements.

| N° | Requirements | Source |
|---|---|---|
| 3.1 | Shall comply with the Telemetry and Tele-command S/C interface requirements. | IID-A |
| 3.2 | Shall comply with the mechanical S/C interface requirements. | IID-A |
| 3.3 | Shall comply with the electrical S/C interface requirements. | IID-A |
| 3.4 | Shall comply with the thermal S/C interface requirements. | IID-A |

Instrument Interface requirements.

| N° | Requirements | Source |
|---|---|---|
| **4.1** | **Shall interface with the instrument subsystems.** | |
| 4.1.1 | Shall interface with the Instrument detectors. | |
| 4.1.1.1 | Shall interface with the Photometer detectors. | |
| 4.1.1.2 | Shall interface with the Spectrometer detectors. | |
| 4.1.2 | Shall interface with the **FTS mirror** moving system. | |
| 4.1.3 | Shall interface with the **Chopper actuator** system. | |
| 4.1.4 | Shall interface with the **Calibration Sources**. | |
| 4.1.5 | Shall interface with the **Cryo-cooler** system | |
| 4.1.6 | Shall interface with the **Shutter** system. | |
| **4.2** | **Shall comply with the instrument mechanical interfaces.** | |
| **4.3** | **Shall comply with the instrument electrical interfaces.** | |
| **4.4** | **Shall comply with the instrument grounding scheme.** | |

Performance requirements.

| N° | Requirements | Source |
|---|---|---|
| **5.1** | **Shall be able to perform Data acquisition.** | |
| 5.1.1 | Shall be able to handle simultaneous data acquisition of the 3 Photometer detectors at a TBD rate with a n bit accuracy. | |
| 5.1.2 | Shall be able to handle simultaneous data acquisition of the 2 Spectrometer detectors at a TBD rate with a n bit accuracy. | |
| 5.1.3 | Shall be able to handle H/K acquisition at a TBD maximum rate with a n bit accuracy. | |
| **5.2** | **Shall be able to accept all Tele-command packets sent at the nominal OBDH transfer rate.** | **OIRD-CTRL-5 OIRD-CTRL-6** |
| | | |
| **5.3** | **Shall be able to send variable length Telemetry packet at a maximum rate of TBD bps and at an average rate of 200kbps.** | |
| | | |
| **5.4** | **Shall be able to process Photometer data at the rate of TBD image per second.** | |
| | | |
| **5.5** | **Shall be able to process Spectrometer data at the rate of TBD per second.** | |
| | | |

Reliability requirements.

| N° | Requirements | Source |
|---|---|---|
| 6.1 | Shall be single point failure resilient. | |
| | | |
| 6.2 | Shall handle cold redundancy capability. | |
| | | |
| 6.3 | Shall able to cope with degraded modes. | |
| | | |

Safety requirements.

| N° | Requirements | Source |
|---|---|---|
| 7.1 | Shall keep the instrument and the S/C interface safe when switched off at any time. | |
| | | |
| 7.2 | Shall keep the instrument and the S/C interface safe when switched on. | |
| | | |
| 7.3 | Shall keep the instrument and the S/C interface safe at any time when operated. | |
| 7.3.1 | The execution of any tele command shall never affect the health of the Instrument. | |
| 7.3.2 | Shall be able to check critical H/K against safety limits. | |
| 7.3.3 | Shall be able to switch off all or parts of the instrument in case of critical H/K safety limit crossing. | |
| 7.4 | Shall perform self-checking. | |
| 7.4.1 | Shall perform regular Instrument health checking. | |
| 7.4.2 | Shall perform Task execution monitoring. | |
| 7.4.3 | Shall perform regular memory checking. | |

Compatibility requirements.

| N° | Requirements | Source |
|---|---|---|
| | | |
| | | |

Quality requirements.

| N° | Requirements | Source |
|---|---|---|
| | | |
| | | |
| | | |

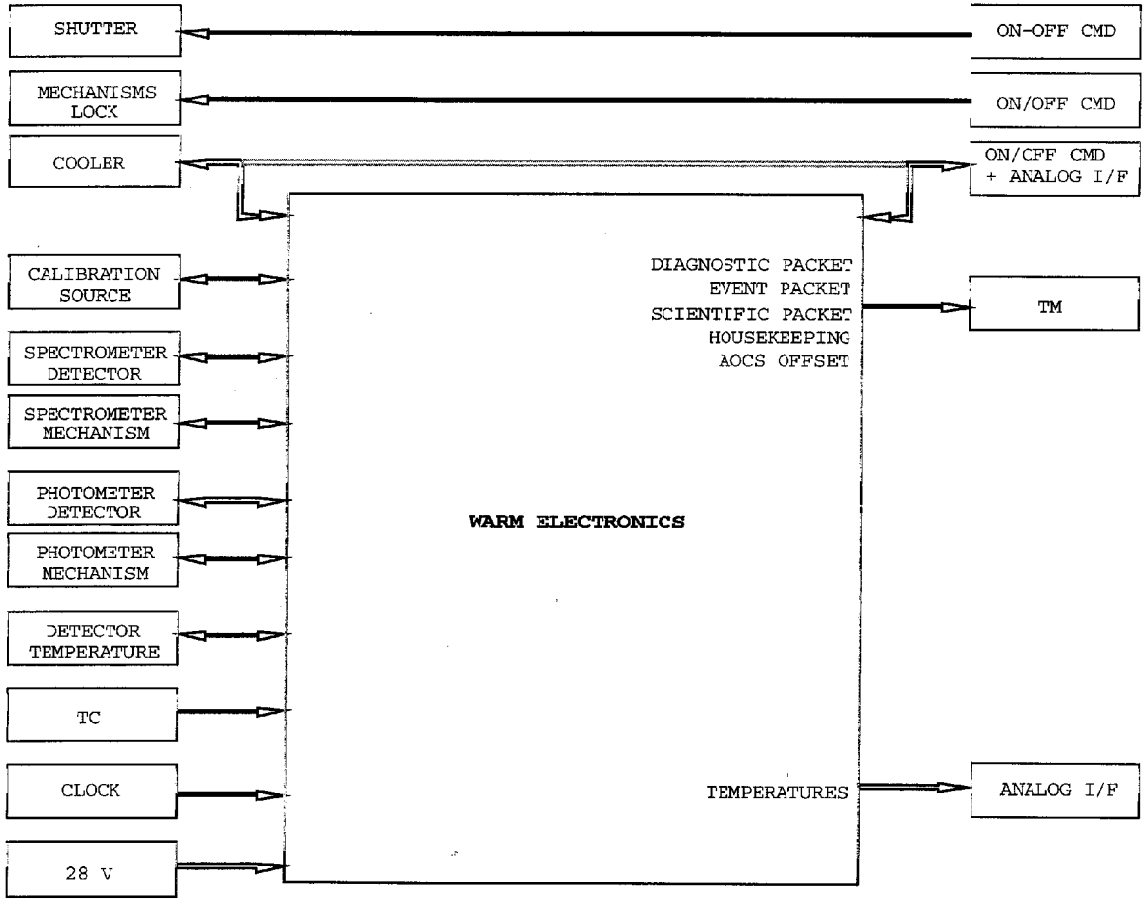
# Products & Tests vs. Models (1)

| | | Resp. | EM | AVM | CQM | PFM | FS | Comments |
|---|---|---|---|---|---|---|---|---|
| **WE UNITs** | | | | | | | | |
| **DPU** | | | | | | | | |
| | **Electronics** | | | | | | | |
| | CPU Board | IFSI | 1 | 1 | 2 | 2 | (2/3) | FS shared with other Inst. |
| | Memory | IFSI | 1 | 1 | 2 | 2 | (2/3) | |
| | Power Supply | IFSI | 1 | 1 | 2 | 2 | (2/3) | |
| | *Component Grade* | | Std | Std | Mil | Qual | Qual | |
| | **Mechanics** | | | | | | | |
| | DPU Box | IFSI | 1 | 1 | 1 | 1 | (1/2) | FS shared with other Inst. |
| | Connectors | IFSI | X | X | X | X | X | |
| | **S/W** | | | | | | | |
| | LL s/w | IFSI | V0 | V1 | V1 | V flight | V flight | |
| | HL s/w | IFSI | V0 | V1 | V1 | V flight | V flight | |
| **SPU** | | | | | | | | |
| | **H/W** | | | | | | | |
| | CPU Board | IAC | 1 | 1 | 2 | 2 | 1 | |
| | Memory | IAC | xMo | xMo | 2*(xMo) | 2*(xMo) | xMo | |
| | Power Supply | IAC | 1 | 1 | 1 | 1 | 1 | |
| | *Component Grade* | | Std | Mil | Mil | Qual | Qual | |
| | **Mechanics** | | | | | | | |
| | SPU Box | IAC | 1? | 1 | 1 | 1 | (1/2) | FS shared with other Inst. |
| | Connectors | IAC | X | X | X | X | X | |
| | **S/W** | | | | | | | |
| | LL s/w | IAC | V0? | V1? | V1? | V flight | V flight | |
| | HL s/w | SAp | V0? | V1? | V1? | V flight | V flight | |
| **DRCU** | | | | | | | | |
| | **Electronics** | | | | | | | |
| | Detector Readout | SAp | 1 | - | 1 | 1 | 1 | |
| | FTS Control | LAS | 1 | - | 2 | 2 | 1? | |
| | Cryo Control | SAp | 1 | - | 2 | 2 | 1? | |
| | Chopper Control | SAp | 1 | - | 2 | 2 | 1? | |
| | Calib. Source Control | SAp | 1 | - | 2 | 2 | 1? | |
| | H/K readout | SAp | 1 | - | 2 | 2 | 1? | |
| | *Component Grade* | | Std | - | Mil | Qual | Qual | |
| | **Mechanics** | | | | | | | |
| | DRCU Box | SAp | 1 | - | 1 | 1 | 1 | |
| | Connectors | SAp | X | X | X | X | X | |
| **BAU** | | | | | | | | |
| | **Electronics** | | | | | | | |
| | Buffers | SAp | 1 | | 1 | 1 | 1 | |
| | Temp. Regulation | SAp | 1 | | 1 | 1 | 1 | |
| | *Component Grade* | | Std | | Mil | Qual | Qual | |
| | **Mechanics** | | | | | | | |
| | BAU Box | SAp | 1 | 2 | 2 | 2 | 1 | |
| | Connectors | SAp | X | X | X | X | X | |
| **Harness** | | | | | | | | |
| | **DPU to SPU** | SAp | 1 | 1 | 2 | 2 | 1 | |
| | **SPU to DRCU** | SAp | 1 | 1 | 2 | 2 | 1 | |
| | **DRCU to BAU** | SAp | 1 | - | 2 | 2 | 1 | |

# Products & Tests vs. Models (2)

| | | Resp. | EM | AVM | CQM | PFM | FS | Comments |
|---|---|---|---|---|---|---|---|---|
| **Simulators** | | | | | | | | |
| **FPU Simulator** | | | | | | | | Developed by CEA/SIG |
| | **Electronics** | SAp | 1 | | | 1 | | |
| | **Mechanics** | SAp | 1 | | | 1 | | |
| **DRCU Simulator** | | | | | | | | |
| | **H/W** | | | | | | | |
| | Station | SO | 2 | 1 | | | | |
| | Elect. Interface | SO | 2 | 1 | | | | |
| | **S/W** | | | | | | | |
| | **Simulation S/W** | SO | 2 | 1 | | | | |
| **Test Facilities** | | | | | | | | |
| **EGSE** | | | | | | | | |
| | Station | Can. | 4 | | | | | |
| | Elect. Interface | Can. | 4 | | | | | |
| **Local Test Unit** | | | | | | | | Developed by CEA/SIG |
| | Station | | 2 | | | | | |
| | Elect. Interface | | 2 | | | | | |
| **Test Facility S/W** | | | | | | | | |
| | OBDH Interface Emulation | SIG | 1 | | | | | Local Test Unit |
| | RTA Common | RAL | 1 | | | | | |
| | RTA Specific | RAL | 1 | | | | | |
| | QLA | RAL | 1 | | | | | |
| | Telecom. Generation Tool | RAL | 1 | | | | | |
| **Tests** | | | | | | | | |
| | **EMC** | | | | | | | |
| | **Thermal Vacuum** | | | | | | | |
| | **Vibration** | | | | | | | |

# SPIRE Warm Electronics - Top Level



**Diagnostic :**

**This mode is defined to investigate anomalies.**
**• A dedicated Diagnostic Data packet will content detector data and a selection of instrument parameters (IRD-Tlm-09).**
**• Transmission rate will be between 0.1 and 1000 times per second (IRD-Tlm-10).**

**→ for instrument parameters located in the DRCU :**

**• each concerned subsystem (FTS control, Chopper control, ...) shall include registers containing digital values of instrument parameters sampled at a predefined rate.**
**• the Low Level Data Acquisition will be in charge of collecting the selected (by TC) instrument parameters at the proper rate to be included by the DPU in a Diagnostic Data packet (1 of 8).**
**• the Low Level Data Acquisition will be implemented by software (in case of DRCU/SPU merging) or by hardware (less flexible)**

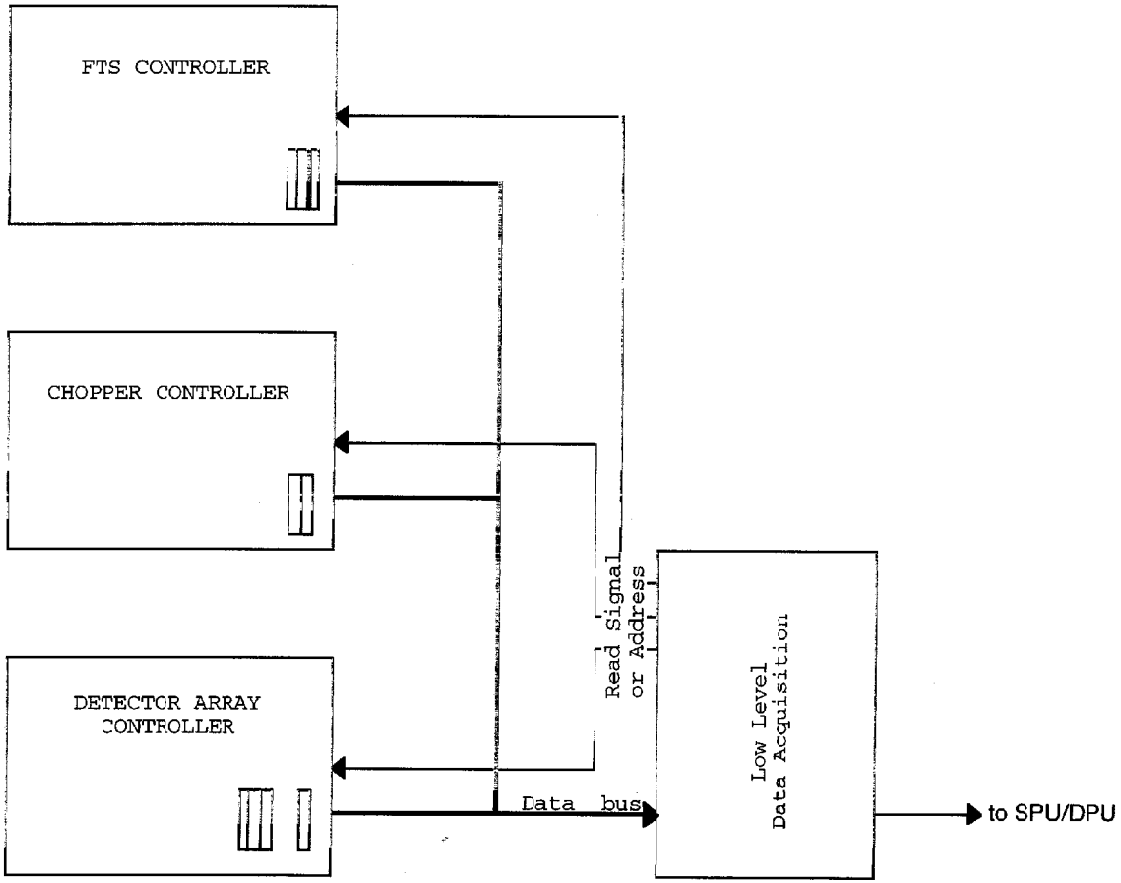
**→ for instrument parameters located in the SPU (parameters of the software) :**

**• the SPU shall merge its own parameters with the parameters transmitted by the DRCU before forwarding an intermediate parameters packet to the SPU via the Scientific Data Interface**

**→ for instrument parameters located in the DPU (parameters of the software) :**

**• the DPU shall merge its own parameters with the intermediate parameters packet transmitted by the SPU**
**• after packing into a Diagnostic Data packet, the DPU transmits the packet to the S/C**

# SPIRE DRCU Detector Data/Parameters Acquisition




6/05/99

# SPIRE Mode of Operation

## Cooler Recycle :

**Cooler recycle is required every 46 hours (TBC) and takes 2 hours.**
**Instead of switching off the instrument it could be useful to optimise the mission to have the possibility to maintain a reduced activity. This activity enables to perform parameter / software tasks upload or download and to perform test.**
**→ In that case for safety reasons it is important to minimise the interaction of this function with the other ones.**

## Real Time Commanding :

**The purpose of this requirement is to enable debugging during ground contact.**

**This mode is not really an instrument mode. It implies the instrument has the possibility to respond "immediately" to TC. This shall be supported by the "Command Execution" function of the DPU.**

**→ This is mainly a S/C mode : in this mode no TM / TC buffering mechanism are activated.**

## Peak-up :

**This mode has to be clarified in order to be able to evaluate the load on the On Board Software. We need the following information**

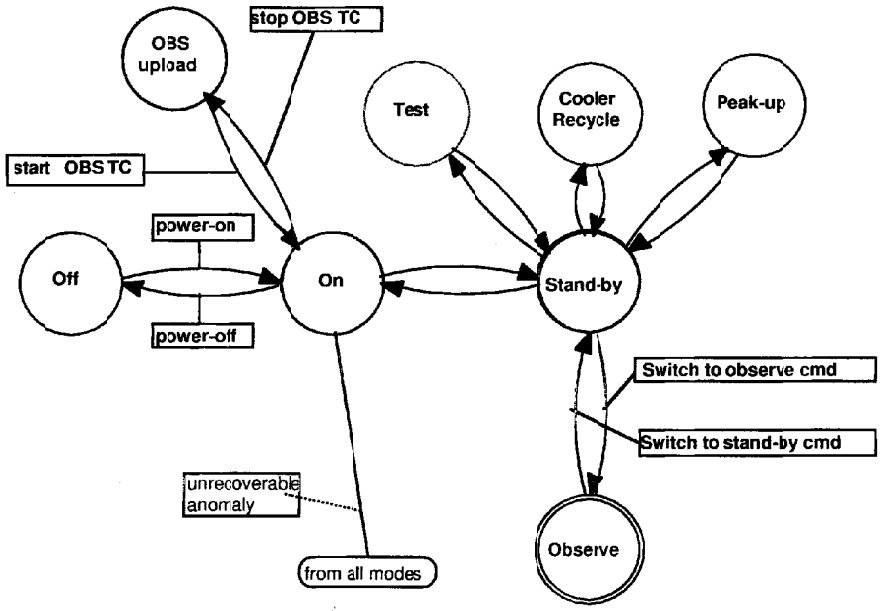
**→ algorithm to be implemented**
**→ rate**
**→ interface with S/C**

## SPIRE Mode of Operation

**Observe :**

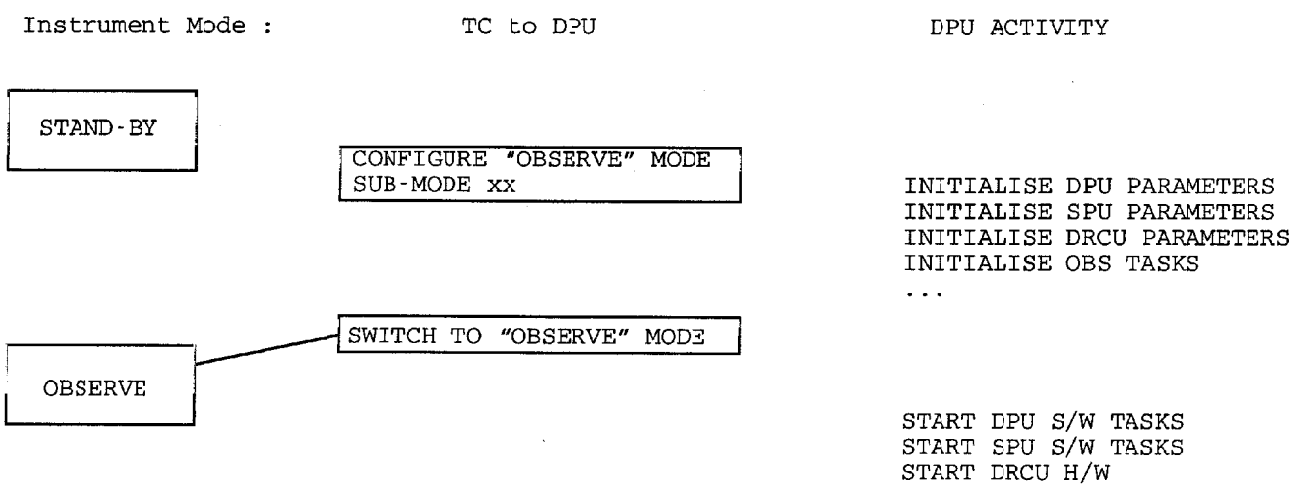
**This mode is divided in to 7 + 3 (spider web and feed-horn option only) sub-modes.**

**This instrument will enter this mode from the standby mode (TBC) :**




**SPIRE MODE SWITCHING**

# SPIRE Mode of Operation




ALL PARAMETERS MAY
- BE DEFAULT PARAMETERS STORED IN DPU PROM
- HAVE BEEN PREVIOUSLY UPLOADED FROM GROUND

PARAMETERS ARE RELEVANT TO THE CONSIDERED OBSERVE xx SUB-MODE ( 1 OF 10)

## TYPICAL MODE SWITCHING SCENARIO

**For some mode/sub-modes the SPIRE Telemetry Rate shall be reduced :**

Sub-modes :

- Partner
- Serendipity
- Parallel

Modes :

- Standby

What do we accept to reduce :

☐ **FOV** - by partial pixel reading of detector arrays

☐ **Spectral Range** - by reading less than 3 detector arrays

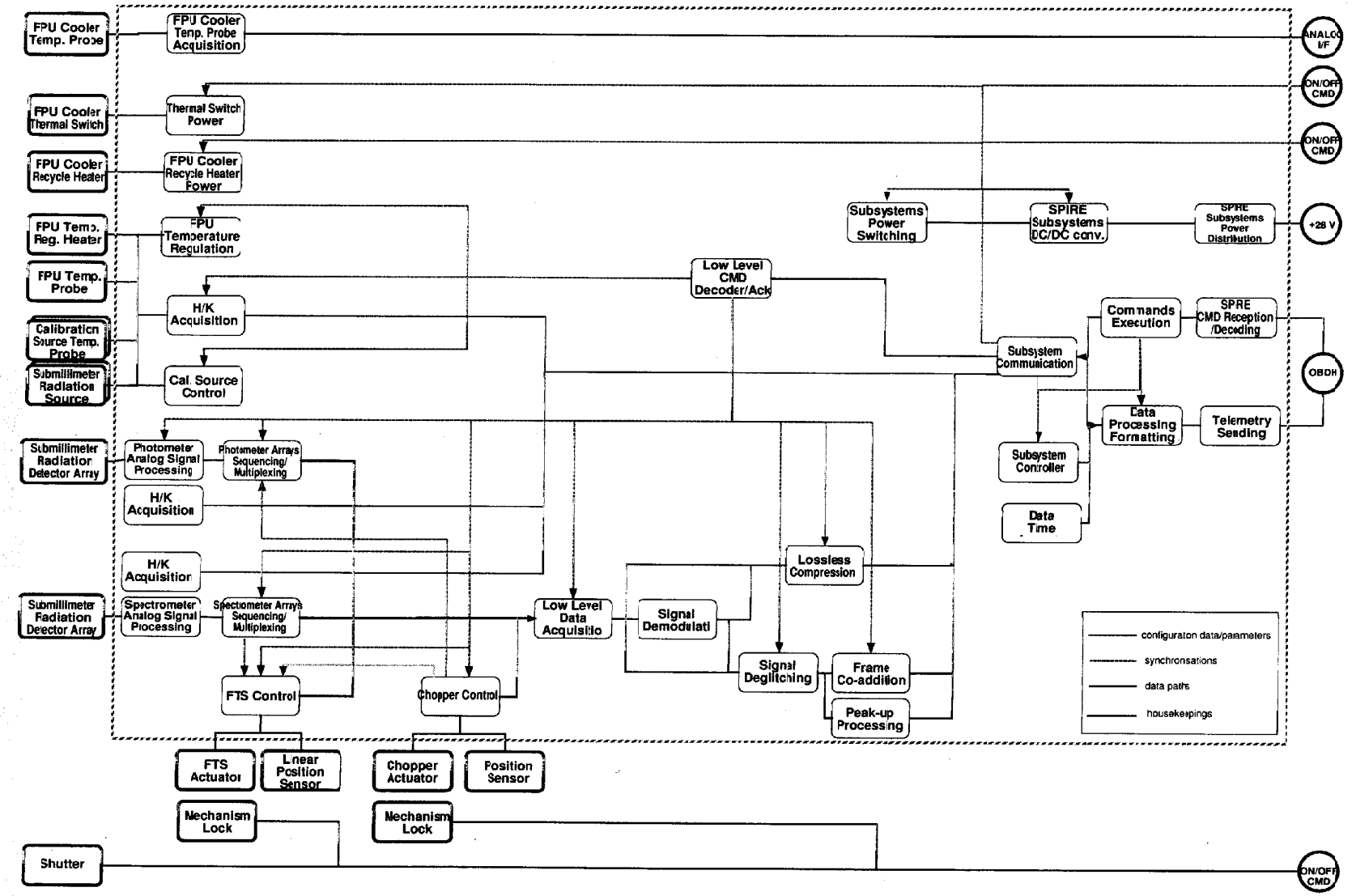
☐ **Image Rate** - by co-adding more images

☐ **Image Rate** - by throwing out images

☐ **A Mix of above**

➔ **Dependently of the choice the impact on instrument functions will be different.**

## WARM ELECTRONICS FUNCTIONNAL BLOCK DIAGRAM



## FUNCTION vs MODE of OPERATION CROSS TABLE (1)

| MODES : | OBSERVE | | | | | | |
|---|---|---|---|---|---|---|---|
| SUB-MODES / FUNCTIONS | Photometer chop | Photometer scan | Photometer. partner | Photometer serendipity | **Photometer parallel** | Spectrometer full | Spectrometer narrow |
| Cooler Recycle Control | No | No | No | No | No | No | No |
| FPU Temp. Regulation | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| H/K Acquisition (Temp.) | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Cal. Source Control | Yes *periodic* | Yes *periodic* | ? | ? | ? | Yes | Yes |
| Photometer ASP | Yes | Yes | Yes | Yes | Yes | No | No |
| Photometer Seq/Mpx | Yes | Yes | *Low Res ?* | Yes | *Low Res ?* | No | No |
| Spectrometer ASP | No | No | No | No | No | Yes | Yes |
| Spectrometer Seq/Mpx | No | No | No | No | No | Yes | Yes |
| FTS Control | No | No | No | No | No | *High Res* | *Low Res* |
| Chopper Control | Yes *Chop* | Yes *Scan* | ? | No | No | No | No |
| Low Level CMD Decoder/Ack | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Data Time Stamping | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Low Level Data Acquisition | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Signal Demodulation | JPL option | JPL option | JPL option | JPL option | JPL option | JPL option | JPL option |
| Signal Deglitching | Yes | Yes | Yes | Yes | Yes | No | No |
| Frame Co-addition | Yes | Yes | Yes | Yes | Yes | No | No |
| Lossless Compression | No | No | No | No | No | Yes | Yes |
| Peak-up Processing | No | No | No | No | No | No | No |
| Subsystem Communication | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| SPIRE CMD Decod. + Exec. | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| Data Processing + Formatting | Yes | Yes | Yes *Low Res* | Yes *Low Res* | Yes *Low Res* | Yes | Yes |
| Telemetry Sending | Yes Full | Yes Full | Yes Partial | Yes TM/2 | Yes Reduced | Yes Full | Full |

- Photometer parallel mode is assumed to be the default standby mode ?
- When applicable the configuration of the function is given in *italic*.

## FUNCTION vs MODE of OPERATION CROSS TABLE (2)

| MODES / FUNCTIONS | Photometer peak up | Jiggle photometer | Jiggle spectrometer | Commissioning Calibration | Diagnostic | Standby | Cooler Recycle | On |
|---|---|---|---|---|---|---|---|---|
| Cooler Recycle Control | No | No | No | No | | No | Yes | No |
| FPU Temperature Regulation | Yes | Yes | Yes | Yes | Yes ? | Yes | No | No |
| H/K Acquisition (Temp.) | Yes | Yes | Yes | Yes | | Yes | Yes | |
| Calibration Source Control | ? | Yes ? | Yes | ? | | No | No | No |
| Photometer ASP[1] | No | Yes | No | Yes | | Yes | No | No |
| Photometer Seq/Mpx | No | Yes | No | Yes | | *Low Res ?* | No | No |
| Spectrometer ASP[2] | Yes | No | Yes | Yes | | No | No | No |
| Spectrometer Seq/Mpx | Yes | No | Yes | Yes | | No | No | No |
| FTS Motion Control | No | No | *Chop. Sync.* | Yes | Yes + *HK* | No | No | No |
| Chopper Motion Control | *Cross raster* | *2D steps* | *2D steps* | Yes | Yes + *HK* | No | No | No |
| Low Level CMD Decoder + Ack. | Yes | Yes | Yes | Yes | Yes | Yes | Yes | *S/W upload* |
| Data Time Stamping | Yes | Yes | Yes | ? | | | | |
| Low Level Data Acquisition | Yes | Yes | Yes | Yes | Yes + *HK* | ? | No | No |
| Signal Demodulation | JPL option | JPL option | JPL option | JPL option | | JPL option | No | No |
| Signal Deglitching | Yes | Yes | No | Yes | | Yes | No | No |
| Frame Co-addition | Yes | Yes | No | Yes | | Yes | No | No |
| Lossless Compression | No | No | Yes | No | | No | No | No |
| Peak-up Analysis | Yes | No | No | No | No | No | No | No |
| Subsystem Communication | Yes | Yes | Yes | Yes | Yes | Yes | No | *S/W upload* |
| SPIRE CMD Reception + Decoding | Yes | Yes | Yes | No limit check | Yes | Yes | Yes | Yes |
| Data Processing + Formatting | *Peak-up* | Yes | Yes | Yes | Yes | *Low Res* | *DPU HK* | *Partial HK* |
| Telemetry Sending | Yes | Yes Full | Yes Full | Yes Full | Yes Full | HK +Data | DPU HK | HK only |

[1] ASP : Analogue Signal Processing

**FIRST/SPIRE**

## SPIRE Acquisition Rates - 4" x 8" FOV

### Photometer

| Central Wavelength µm | Theorical array sizes | Practical array sizes | Number of pixel | Acquisition rate rate Hz | Number of acq. /s | Number of bits | Data rate bits/s |
|---|---|---|---|---|---|---|---|
| 250 | **32x64** | 32x64 | 2048 | 40 | 81920 | 14 | 1146880 |
| 350 | **24x48** | 32x64 | 1152 | 40 | 46080 | 14 | 645120 |
| 500 | **16x32** | 16x32 | 512 | 40 | 20480 | 14 | 286720 |
| | | | | | | Total (average) : | 2078720 |

Minimum compression factor compared to 40 kbits/s (**200 kbits/s**-TBC) : 52 (**10**) → **Image rate** = 1.5 /s (**4 /s**)
Real compression factor will take into account data format (i.e. 3 bytes / pixel)

### Spectrometer

| Wavelength µm | Theorical array sizes | Practical array sizes | Number of pixel | Acquisition rate rate Hz [1] | Number of acq. /s | Number of bits | Data rate bits/s |
|---|---|---|---|---|---|---|---|
| 200-300 | **16x16** | 16x16 | 256 | 40 | 10240 | 14 | 143360 |
| 300-600 | **12x12** | 16x16 | 144 | 40 | 5760 | 14 | 80640 |
| | | | | | | Total (average) : | 224000 |

1 : Assuming a 2 time oversampling

Minimum compression factor compared to **40 kbits/s** (200 kbits/s-TBC) : **6** (1.12 !) → **Interferogram rate = 1 / 240 s**
Real compression factor will take into account data format (i.e. 3 bytes / pixel)
We also have to take into account the duty cycle of the FTS mechanism : assuming 1/10 of time for fly-back compression is no more needed

# SPIRE Analogue Signal Processing Output Rates (JPL Option)

**Photometer :**

| Focal Plane Configuration | Number of pixel | Pixel Sampling Rate (Hz) | Number of Bits | Data Rate (16-bit words/s) | Data Rate (bits/s) |
|---|---|---|---|---|---|
| FOV = 4 x 4<br>2Fλ feed-horn | 117 | 10000 | 16 | $1.2\ 10^6$ | $18.7\ 10^6$ |
| FOV = 4 x 8<br>1Fλ feed-horn | 468 | 10000 | 16 | $4.7\ 10^6$ | $74.9\ 10^6$ |

**• Even if DRCU and SPU interface with parallel data transfer (16-bit words) the data rate of the "468 pixels" option can't be supported by a microprocessor clocked at 10 or 20 MHz (even if it's a DSP !).**

➔ **DATA RATE REDUCTION IS MANDATORY !**

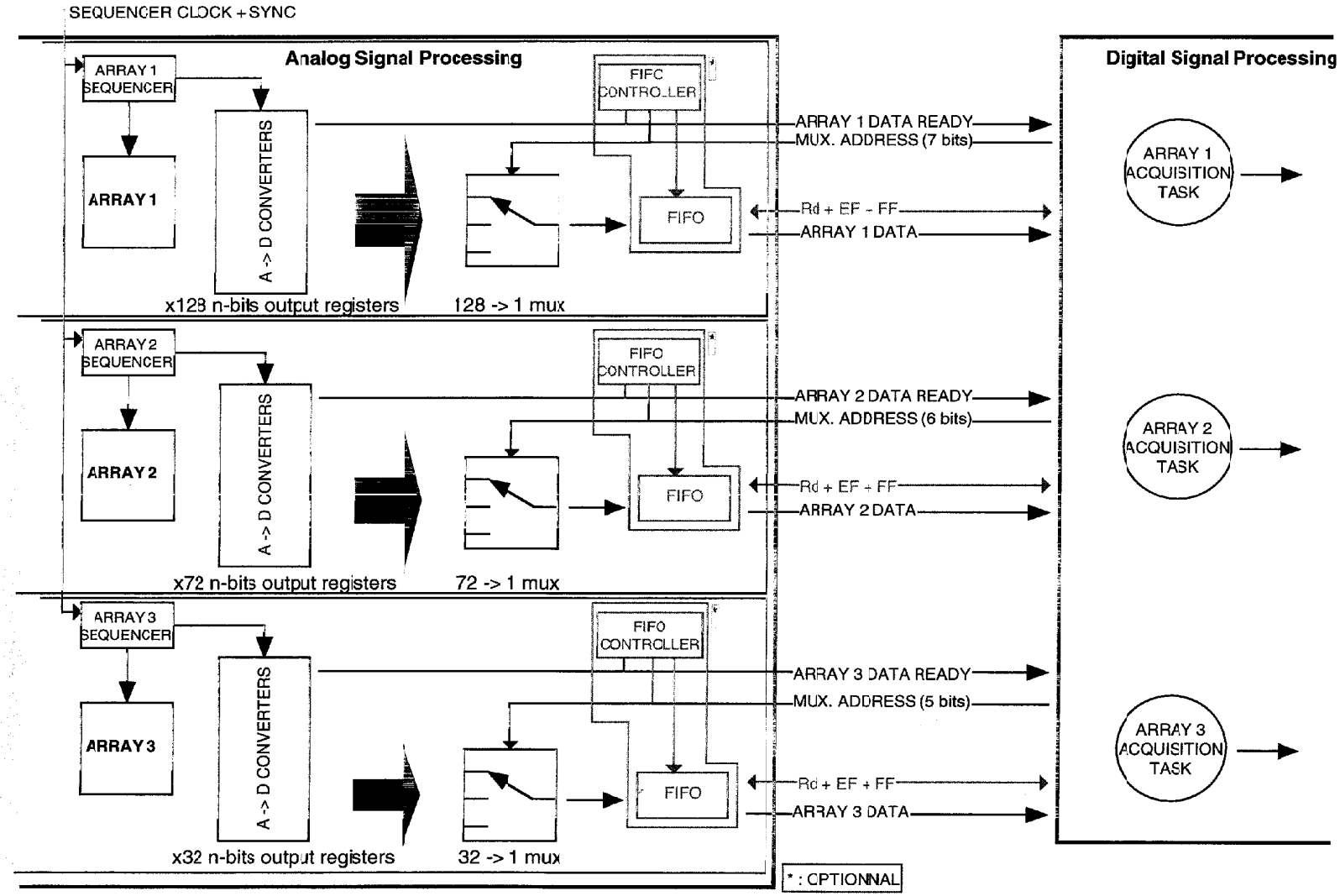
**Solutions to be investigated :**

☐ **Reduction of the oversampling (in that case the demodulation is still implemented by software)**

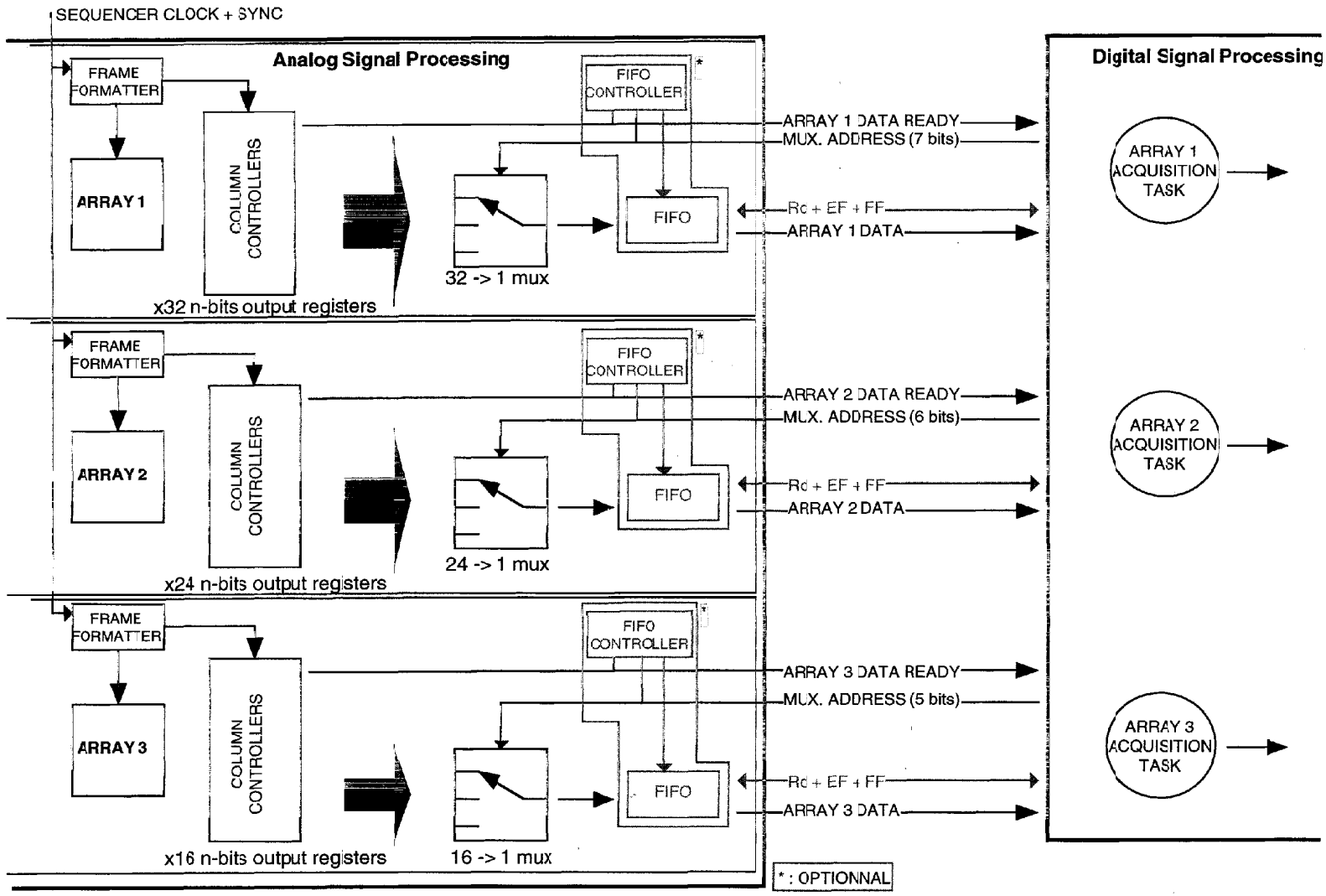
☐ **Demodulation is performed analogically is the analog signal processing**

☐ **Demodulation is performed digitally by hardware (based on FPGA) is the analog signal processing**

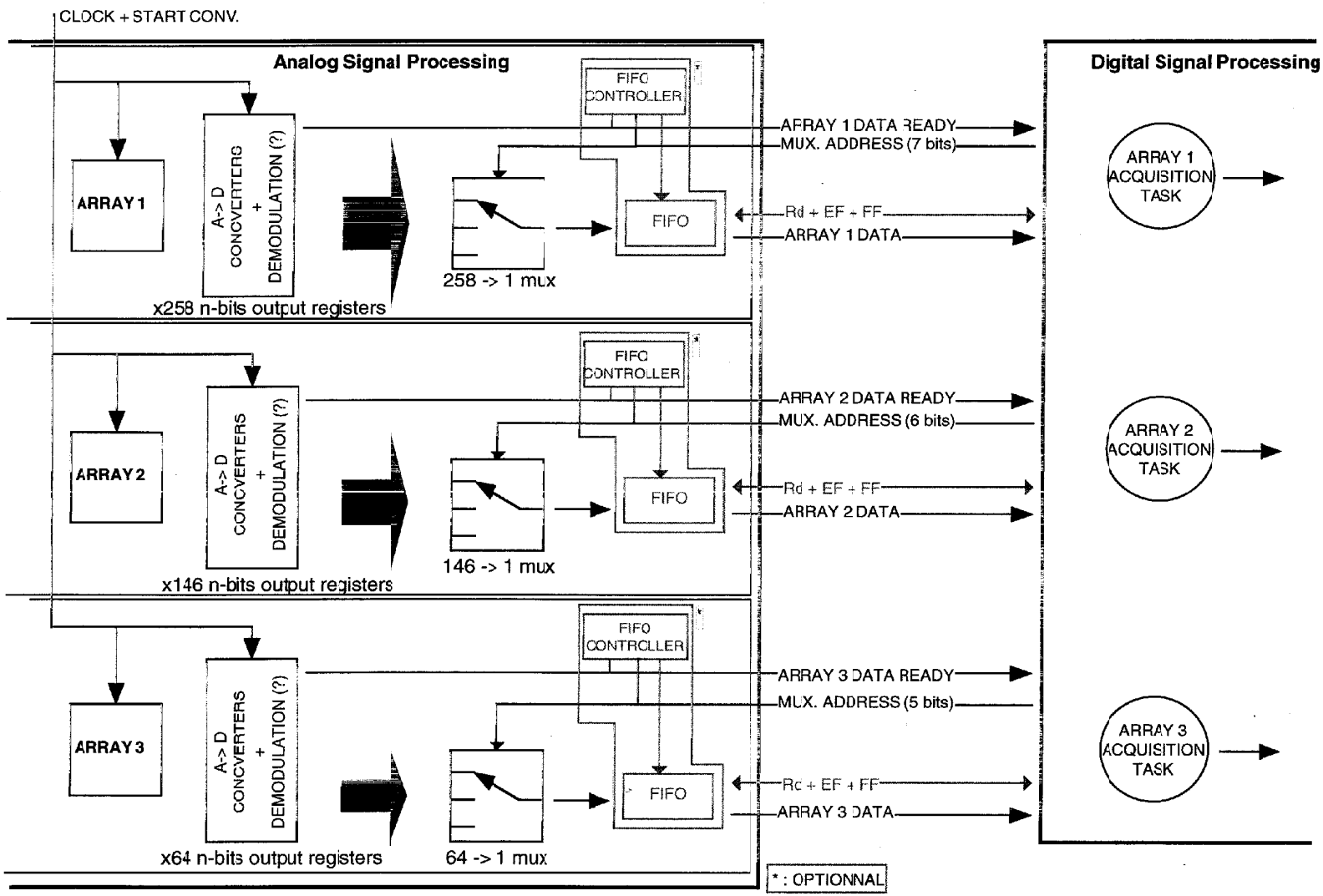
**Analog to Digital Signal Processing Interface - Functionnal Diagram**
**(Photometer - CEA option)**



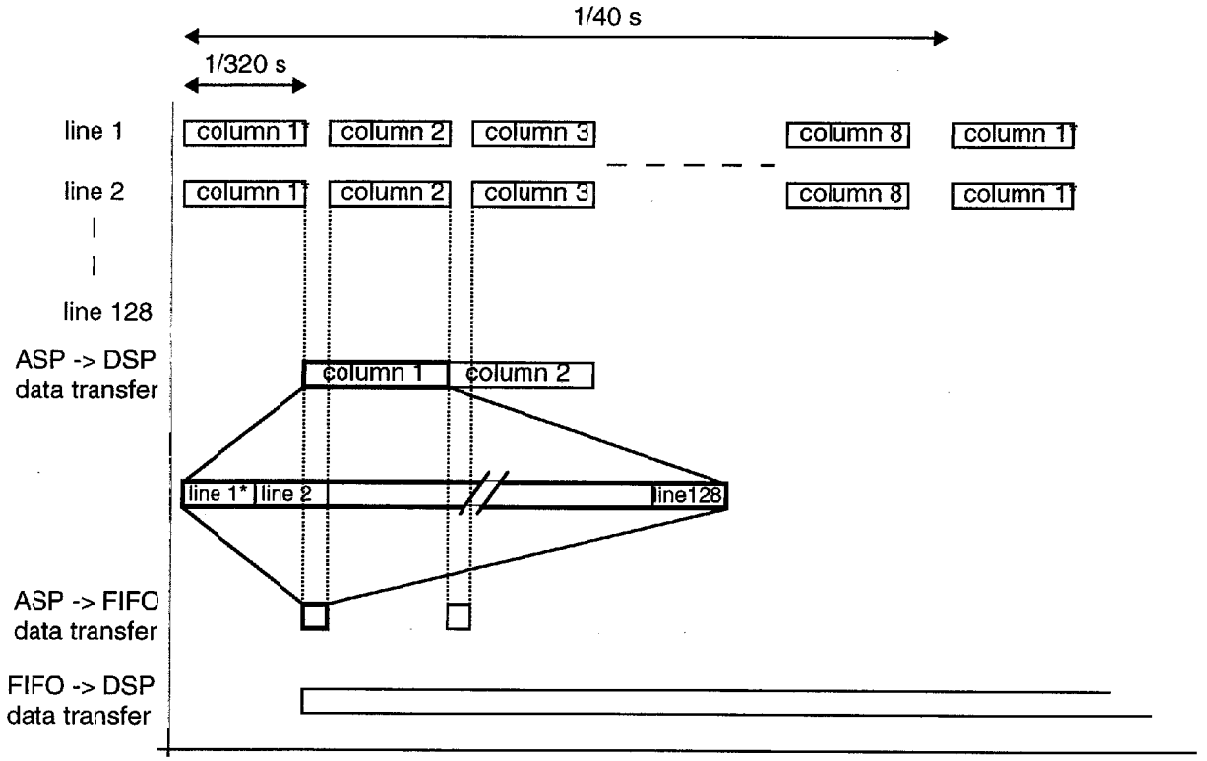
**Analog to Digital Signal Processing Interface - Functionnal Diagram**
**(Photometer - GSFC/NIST option)**



**Analog to Digital Signal Processing Interface - Functionnal Diagram**
**(Photcmeter - JPL option)**



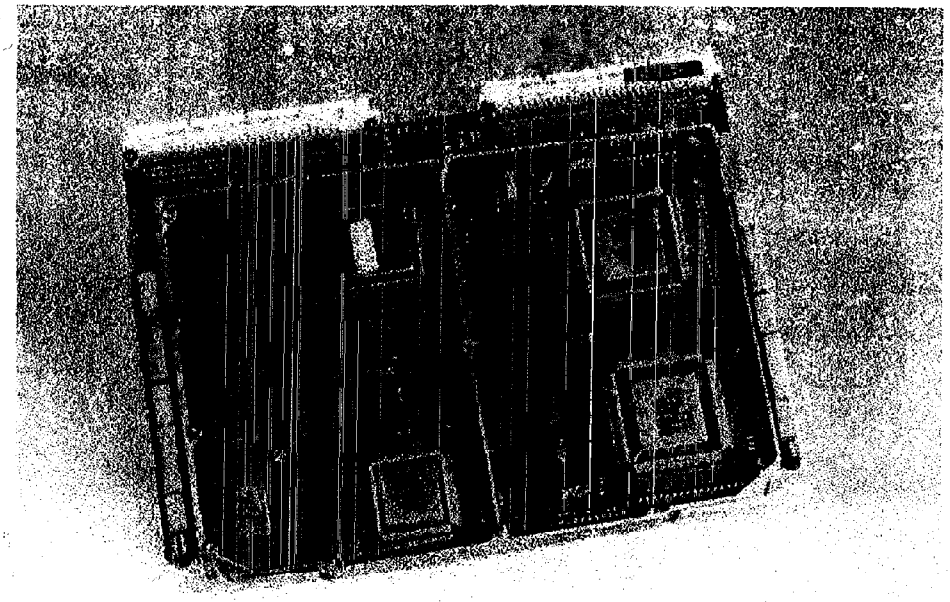
## Analog to Digital Signal Processing Interface - Timing
## (Photometer - CEA Option)




* : frame/line synchro flag associated to pixel data by array sequencer

MATRA MARCONI SPACE

# COMMON PROCESSOR BOARD



MATRA MARCONI SPACE developed in the frame of the COLUMBUS programme a Common Processor Board (CPB). This board is a VME board which provides the central processing capability to on-board computers for space applications.

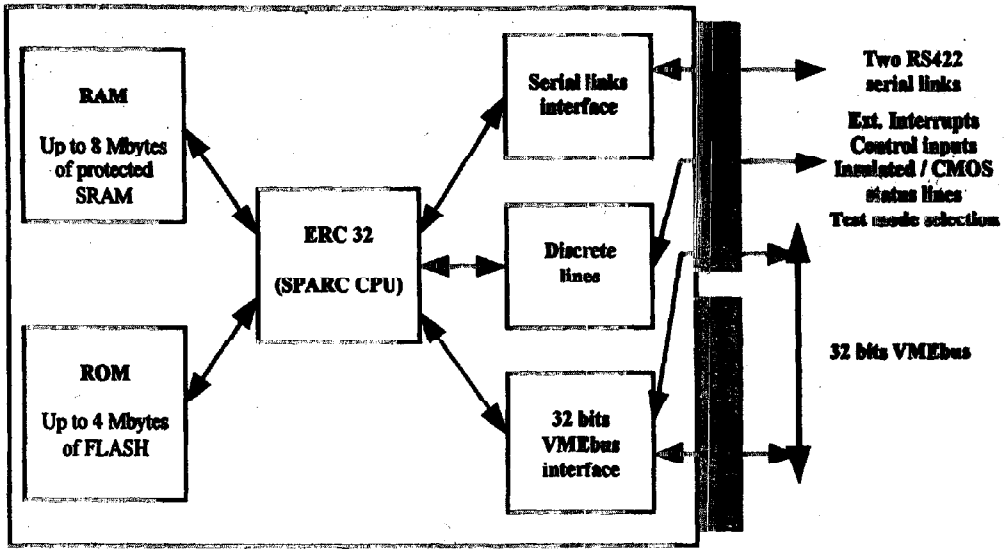
The CPB is based on a SPARC™ architecture. It is typically used as the slot 1 system controller of a VME computer but can also be configurated to operate as a VME master for multiprocessing applications.

Its RAM is protected by Error Detection And Correction. The FlashPROM includes a boot firmware and can be user-programmed to store additional application software. The CPB can be provided with different RAM/PROM configurations.

The CPB is supported by a commercial off-the-shelf real-time POSIX operating system with a C and Ada cross-development environment.

*MATRA MARCONI SPACE*
*37, Avenue Louis Bréguet – BP N°1*
*78146 Vélizy-Villacoublay cedex – France*

OCTOBER 1998




*CPB Block diagram*

## TECHNICAL FEATURES

| | | |
|---|---|---|
| Microprocessor | : | Radiation tolerant ERC32 chip set, compatible with SPARC™ v7 |
| Memory | : | 2, 4 or 8 Mbytes SRAM protected by EDAC<br>1, 2, 3 or 4 Mbytes FlashPROM |
| Performance | : | 9 MIPS Integer / 2 MFLOPS |
| VME Interface | : | IEEE/ANSI std 1014-1987 compliant<br>VME system controller : master, power monitor, bus timer, interrupt handler, bus arbiter, IACK daisy-chain driver.<br>Supports A24:A16 / D32:D16:D8 data transfer modes. |
| Serial Interface | : | 2 x EIA-RS-422 serial ports (9600 bps) |
| Operating system | : | Real time OS32, based on vxWorks™ v5.3.1 |
| Software development environment | : | Tornado™ v1.0.1 |
| Power | : | +5V, typ. 2A / +12V, typ 0.04A (for FlashPROM reprogramming). |
| Mechanical | : | 6U VME conduction cooled board |
| Mass | : | < 600g |
| EEE part quality level | : | MIL-B or equivalent |
| Reliability | : | Failure rate < 6000 fits (MIL-HDBK-217F, Notice 1, SF environment, average PCB temperature = 55°C) |

### 3.2. Functional requirements

#### 3.2.1. ERC 32

The ERC 32 block shall use the SPARC chips set which are the Integer Unit (IU), the Floating Point Unit (FPU) and the MEmory Controller (MEC) [AD3 to AD5].

The ERC32 processing clock frequency shall be of 14 MHz.

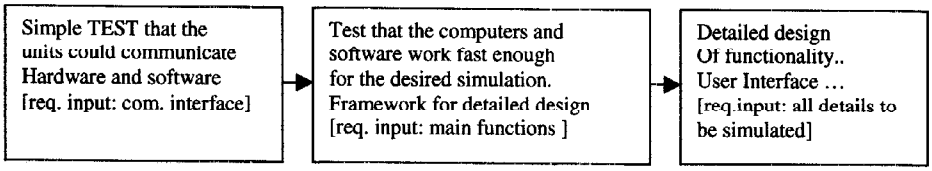
Note that the ERC32 is compatible with SPARC standard Version 7 [RD3], that is it supports 8/16/32/64 bits exchanges.

In addition the MEC will provide the necessary support such as :

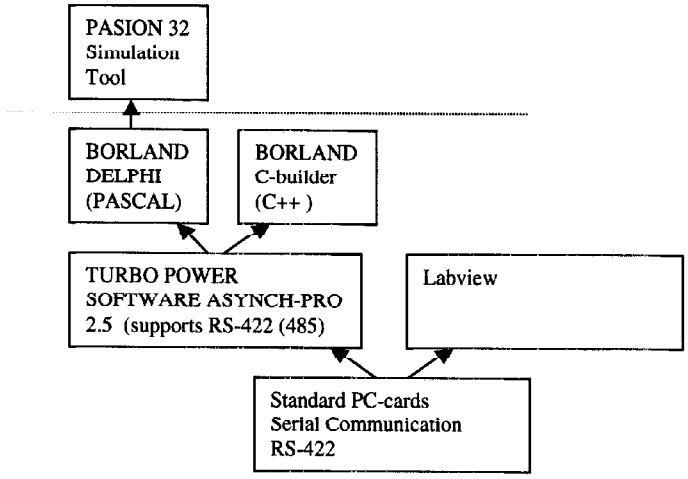
- Memory control and protection,
- EDAC function,
- General purpose timer (resolution : 71 ns to 4.6 ms, Max time : 306 s to 232 days) (note 1),
- Timer (resolution : 71 ns to 18 µs, Max time : 306 s to 21 hours) (note 1),
- Programmable watch dog function (18 s maximum duration with a watchdog clock of 875 KHz (i.e. 14 MHz divided by a 16 prescaler)) (note 1),
- Programmable wait state generator,
- System Clock generator.
- DMA interface,
- Interrupt controller,
- UART function with two serial channels.

Note 1: figures are based on ERC32 processing clock frequency of 14 MHZ.

## Rough plan for Simulator development -Stockholm Observatory



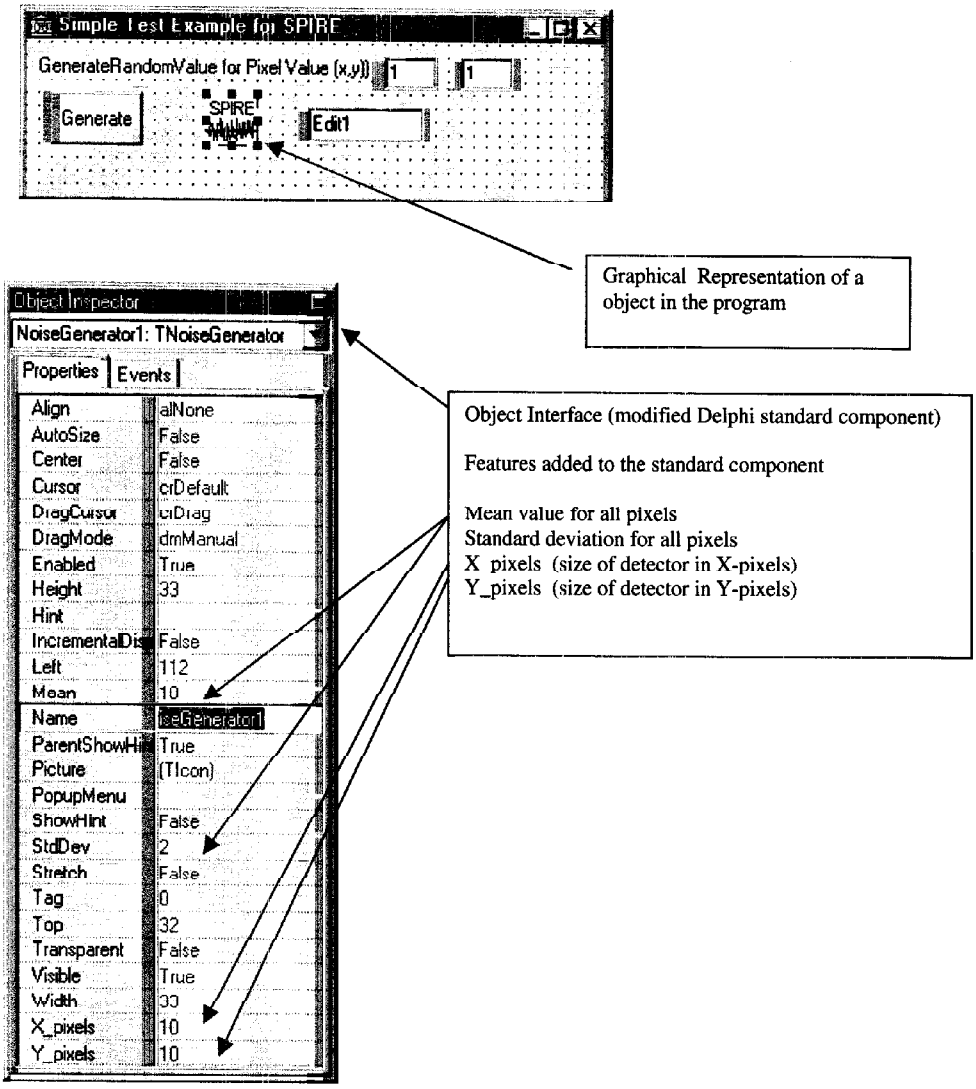

## Possible chain of software (simulator)




## Software links for updated information

| | |
|---|---|
| **Async Professional (general)** | http://www.turbopower.com/products/apro |
| **RS-485 (422)** | http://www.turbopower.com/products/apro/rs485 |
| **Delphi (pascal)** | http://www.borland.com/delphi |
| **C++ Builder** | http://www.borland.com/bcppbuilder/ |
| **References DELPHI as simulation tool [Page 2 bottom]** | http://www.nlr.nl/public/facilities/f141-01/ |
| **Labview** | http://www.natinst.com/labview |
| **Pasion ( top layer simulation tool) (could be compiled in DELPHI) [no experience using it]** | http://www.raczynski.com/pn/sumduz.htm |

# A simple test example of a component based program in DELPHI




**Stockholm Observatory**
**H-G Florén**
**Phone : +46-8-164484**
**Fax : +46-8-7174719**
**e-mail:** florcn@astro.su.se