Long, JA (Judy)

From: AUGUERES Jean-Louis DAPNIA[SMTP:AUGUERES@DAPNIA.CEA.FR]
Sent: Friday, February 19, 1999 1:57:06 PM
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'milena@sirius.ifsi.rm.cnr.it'; 'anna.digiorgio@ifsi.rm.cnr.it'; 'luigi@ifsi.rm.cnr.it'; 'saraceno@ifsi.rm.cnr.it'
Subject: Draft minutes of the IFSI / SAp meeting - Feb. 16, 1999 at IFSI
Auto forwarded by a Rule

Dear all,

Please find attached the draft minutes of the IFSI / SAp meeting.

Waiting for your comments.

Cheers,

Jean-Louis

PS. I will be away next week.

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DRAFT Minutes of the SAP/IFSI meeting.
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IFSI, Feb. 16, 1999

Attendees:

  IFSI : Ricardo Cerulli, Renato Orfei, Stefano Pezzuto,
         Milena Benedettini, Anna-Maria Di Giorgio,
         Luigi Spinoglio, Paolo Saraceno
  SAp   : Jean-Louis Augueres, Christophe Cara
  RAL   : Ken King

1.   IFSI situation. (see IFSI VGs)

        The presentation was made by RC.

  1.1 Involvement and situation regarding the other FIRST/Planck
     instruments.

  IFSI is committed to provide the DPUs of the 3 FIRST instruments.

  1.2 Funding issues.

  Although ASI has given the first priority to Planck's LFI, IFSI
  does not expect major problems.

  Extra manpower shown in the Cost breakdown table is funded by ASI.

  1.3 Working organization and manpower.

  Reported in IFSI VGs.

1.4 Current developments.

DPU status reported in IFSI VGs.

S/C interfaces are discussed in the framework of CWG#2.

2. Overall WE SPIRE electronics architecture.

See SAps'VGs.

2.1 Overall architecture.

The chopper electronics is missing on the overall diagram (it will be amended).

IFSI stressed that the local test unit should interface with the DRCU rather the SPU.

SAp agreed that the both situations have to be considered. In the case where the SPU is suppressed, the only remaining interface is with the DRCU anyway.

2.2 WE subsystems interconnection.

CC presented, as a proposal for discussion, a diagram showing the various links between the WE electronics boxes (communication links and power supply) including redundancy aspects. The baseline case (DPU+SPU) and Single processor case (DPU only) have been presented.

IFSI noticed that contrary to what is shohn on the VGs, the ESA baseline is to have one DC/DC per box.

2.3 Incidence of array options.

CC presented a diagram showing the impact of the 3 competing options (decision to be made in Jan. 2000). Apart from the fact that the readout electronics differ substantially, the main impact on the CPUs is that the estimated data throughput varies from 1.9 Mb/s (CEA option) to 1 Gb/s TES option).

Data processing (mainly the necessary compression to keep the average data throughput below the average telemetry rate allowed) are still TBD

2.4 Model definition.

The ISFI point of view is summarized on a VG.

CC presented a VG (attached) showing a proposal based on the SAp understanding on the ESA requirements.

AVM:

The AVM aims to check the OBDH to S/C interface. The necessity to have a representative SPU is not obvious. DPU to SPU interface could be simulated (h/w or s/w).

IFSI state that the AVM concept aims to froze the h/w while the s/w may be upgraded.

SAp think that it could be true as far as the s/w modification have no impact on S/C interface.

KK questioned about the availability of a breadboard model before

the delivery of the AVM.

This question have to be discussed in the framework of the DPU development plan.

EQM:

IFSI pointed out that they intend to produce an EQM: similar to the DPU AVM model + redundancies (see the HIFI model philosophy VGs (on this VG ICU means DPU)).

CQM:

IFSI propose to use the AVM as part of the CQM.

SAp position is to keep the CQM as simple as possible and did not foresee to deliver the DPU as a part of the CQM as their understanding of the CQM goal was not to demonstrate that the whole chain is working end to end but to focus on optics, mechanics, detector, readout electronics.

SAp however agree that this could be determined only when a development plan accompanied by a development flow diagram and an accordingly detailed schedule will be available.

Everybody agree that the first priority has to be given to the production of the above documents. It will be the top goal of the discussion of the next (and first) WE Group meeting.

AI #1 - KK to provide asap a reasonably stable version of the SPIRE development plan (including schedule and a flow diagram).

JLA stressed that it could be a difference between what ESA is requiring and what we need for I&T and calibration purpose in the various labs at different stages. The delivery of non requested items will imply additional workload and cost (documentation production, additional I&T efforts, duplication of unnecessarily delivered item for our own use,...)

IFSI emphasized that if the CQM does not include the DPU, the working of the whole chain will only be demonstrated with the PFM.

PFM:

No comment.

FS:

IFSI position is the delivery of spare boards (on the same line of the SPIRE project). This is however not the ESA baseline.

3. Managerial issues.

  3.1 SPIRE Instrument Development plan.

The SPIRE Instrument development plan document prepared by KK (available as a very preliminary draft) has been handed out for comment.

AI #2 - IFSI and SAp to send comments to KK by March 15.

3.2 Overall SPIRE schedule.

The overall schedule based on the official ESA milestones as been

presented and discussed. The SAp have made a proposal more compatible with SAp funding by CNES. Discussions still ahead.

The "waterfall" development put constraints on both AVM and CQM development which have to be ready before the start of the PFM implementation.

There is no SPIRE schedule available at the model development level (it depend on the development plan (model policy + AIV)).

3.3 Comparison with other instrument schedules.

IFSI pointed out that the other instruments have similar overall development schedules.

IFSI stressed that when it comes to AVM, the specifications have to be ready by July 99.

2.3 Warm electronics unit management (responsibility, co-ordination, reporting)

The WE management scheme has been clarified and agreed at the last Consortium meeting. (see the SPIRE management plan).

The WE activity is one of the Development Unit under the responsibility of the WE Unit manager (JLA).

Local PM report both to KK and the Unit manager.

KK said that the reports to ESA are based on the Unit reports which have to summarize the information from the local PM reports. These reports will be available (the first one being already) on the DMS SPIRE public domains.

Individual reports from the local PM are available on the DMS SPIRE internal domain.

CC is responsible for the overall electronics design and development.

A WE Group is defined. It encompasses permanent members of the main institutes contributing the electronics development (SAp, IFSI, IAC, LAS, SO) and other people (as circumstances require) (see minutes of the Consortium meeting).

IMPORTANT:

The proposed date for the first WE Group meeting is March 24-25, 1999 at Saclay.

AI #3 - SAp (JLA) to issue a proposal agenda by March 15, 1999.

3.4 DPU development plan and needs for electronics prototypes, AVM, CQM, FM & FS.

IFSI presented a high level development schedule for the AVM (see VG).

According to this schedule, the DPU AVM specification should be ready by early July 99.

3.5 DPU delivery milestones (prototypes, AVM, CQM, FM, FS).

IFSI stated that the DPU AVM delivery (to SAp) goal is Jan. 2001. This milestone is constrained by the test of the CQM.

3.6 Commonality issues (participation to CWGs).

See VGs.

IFSI participate in CWGs #2, #3, #4, #5 as cross instrument support.

4. System issues.

4.1 DPU/SPU versus DPU alone.

This question has been extensively discussed.

Two options are considered:

a) the original baseline option (DPU + SPU (+DMA?))
b) the alternative option: DPU + additional memory (IAC provided)
            + DMA?

Arguments exchanged will not be reported in these minutes. By and large, IFSI was the DPU/SPU baseline version defendant, SAp arguing in favor of the DPU alone solution (RAL (KK) keeping a positive neutral attitude).

Given the importance of the subject and in order that pro and cons (in term of cost, schedule, manpower, budget, reliability,...) could be examined with the best possible objectivity while allowing all parties to express themselves it as be decided to produce a note. JLA suggested that this note should have an "objective" part (as a table summarizing the various domains and listing as objectively as possible the pro and cons) and a contradictory part where each part could give their own interpretation.

The final document will be discussed at the March WE Group meeting. The group will then issue (if necessary) their recommendations and eventually leave the decision to higher authority (System group, Steering group,...).

AI #4 - JLA to issue by March 10, 1999 the first draft of the note on the DPU/SPU vs. DPU alone choice.

4.2 S/C interface.

This is considered in the framework of the CWG #2.

ESA documentation is awaited.

R.Orfei, R.Cerulli, J.Herreros (IAC - to be confirmed) and C.Cara will attend the CWG #2 kick off meeting to be held in ESTEC on March 3, 1999.

Command format, capabilities and handling are under discussion (see VGs).

KK stated that, due to the slow uplink telecommand uplink, the volume of commands has to be minimized (use of macro).

S/W up-loading has to be optimized as well.

4.3 Grounding and bounding scheme.

IFSI presented the HIFI grounding scheme based on the distributed single point.

4.4 Mass & power budget.

Seems not to be a critical issue at DPU level.

4.5 SPU / DRCU interface.

See SAp VG and considerations about the throughput stemming from the different detector options.

5. Qualification program (thermic, vibration, EMI/EMC)

IFSI stressed that the DPU qualification could be carried out once for all the 3 instruments.

6. Components.

6.1 Micro-processor (DSP vs. SPARC)

The DSP is the baseline. This is stemming from:

- the availability of qualified component.
- the pre-existence (Laben) of a similar CPU board.

However, both SAp and IFSI would prefer to use a SPARC processor. The rationale is manifold. Among others:

- the SPARC offer a better adaptation to deal with Real time s/w.
- development s/w are widely available and are more user-friendly.
- ...

A drawback however:

- the availability of a space qualified version is to be confirmed.

AI #5 - ISFI & SAp to raise the DSP vs. SPARC issue at the March 3 CWG #2 meeting.

6.2 Communication channels.

A rough computation demonstrate that even if the slowest throughput is considered and given the real time constraints, the use of a DMA is compulsory (for the SPU and/or the DPU).

This issue will be raised at the next CWG #2 meeting (March 3).

AI #6 - ISFI & SAp to raise the DMA issue at the March 3 CWG #2 meeting.

7. QA issues (H/W & S/W).

7.1 H/W.

Concerning the CPU board IFSI state that it should be bought from Laben and therefore fully qualified.

The interface board will be built by IFSI according to ESA standard. The qualification tests will be performed as per the IID-A.

KK stated that a QA document for SPIRE subsystems is expected from the SPIRE PA manager.

7.2 S/W

IFSI emphasized that the s/w will be developed according to ESA

PSS05 - lite.

8. S/W issues.

8.1 Requirements.

The question of the writing of the User requirements for the DPU
s/w lead to the observation of the necessity to get first the
overall SPIRE System requirements.

The WE group should contribute to the writing of the DPU user
requirements. A custodian (and responsible) have to be appointed.

KK stressed that the User requirements have to be reviewed at the
SPIRE PDR (Sept. 99).

8.2 Overall DPU s/w architecture

An overall s/w architecture has been presented by ADG (see VGs).

About the "SPIRE O/B s/w contect diagram", JLA stressed that (in
the case that the DPU/SPU baseline is kept), the direct handling
of the instrument housekeeping could be an issue as it is expected
that some of the housekeeping parameters are needed at SPU level.

On the logical model, it has been remarked that there is "a
priori" no reason to treat differently the Memory dump command.

JLA stressed that given the kind of processor envisaged, the CPU
power needed to deal with these activity should not exceed a few
percents of the total CPU power available.

8.3 Development tools.

Should be available.

8.4 Real-time OS.

The baseline is Virtuoso (see IFSI evaluation VG). Ongoing
evaluation by a Planck team.

A home made Real-Time kernel (to be developed) is envisaged by
IFSI.

9. DPU architecture (including redundancies).

9.1 Overall DPU architecture.

Presented by IFSI (see VG) on the basis of the DSP.

A DMA has to be implemented.

9.2 Required resources.

See IFSI VG.

10. I&T issues.

See IFSI VG.

Action List:
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AI #1 - KK to provide asap a reasonably stable version of the
        SPIRE development plan (including schedule and a flow

diagram).

AI #2 - IFSI and SAp to send comments to KK by March 15.

AI #3 - SAp (JLA) to issue a proposal agenda by March 15, 1999.

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CWG #2 meeting.