March 24th Agenda

Wednesday 24 - meeting start 9.30

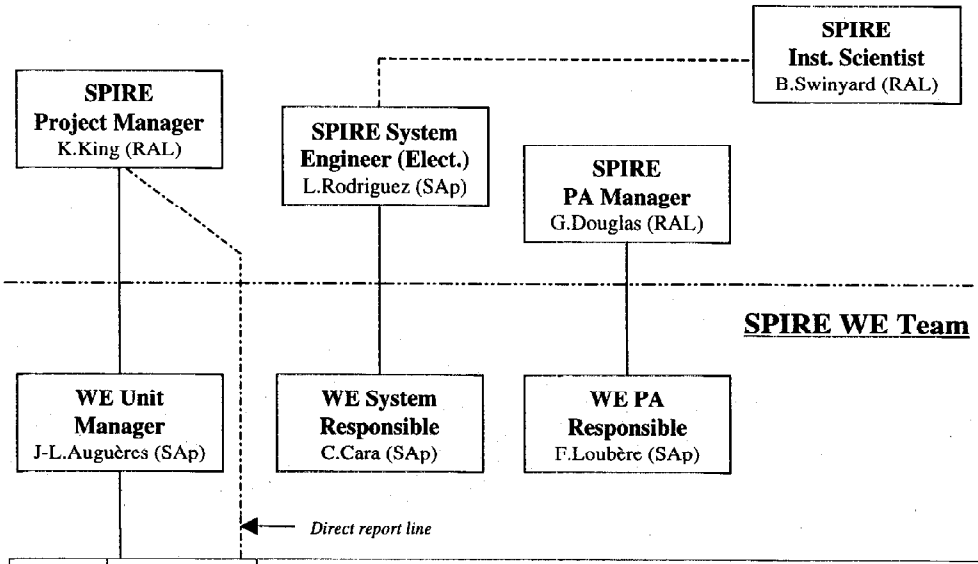
9.30	Review of the agenda of the meeting.	JLA	10'
9.40	Managerial issues		
	- SPIRE organisation	KK	5'
	- Schedules (short & long term)	KK	15'
	- Organisation of the WE team. (work sharing, interfaces, reporting, participation to the CWGs, WE meetings)	JLA	15'
	- Action review	JLA	5'
	- Status of the institutes (short presentation on managerial issues)	all POCs	5' each
10.40	Coffee break.		
11.00	Warm Electronics requirements and constraints.		
	- Review of existing requirements and shade areas (missing parameters and requirements).	CCa	40'
	- WE Budgets	CCa	10'
	- S/C Interfaces	IFSI	20'
	- Commonality issues	KK	20'
12.30	Development plan.		
	- SPIRE development plan	KK	15'
	- WE development plan (discussion on ESA WE model policy, development models, test facilities.)	JLA	15'
13.00	Lunch		
14.00	WE Quality Assurance. (Plan & Organisation)	SAp/FL	30'
14.30	Warm Electronics design.		
	- Overall architecture (discussion on the DPU/SPU options)	CCa	45'
	- Detector technology impact.	CCa	20'
	- Redundancy issues.	CCa	30'
	- Power supply and grounding scheme	RC	20'
	- Part list.	CCa,VM	15'
17.00	End of the first day.		

March 25th Agenda

Thursday 25 - meeting start 9.30

9.30	Subsystem development.		
	- DPU		
	. h/w	IFSI	20'
	. s/w functionality	IFSI	20'
	- SPU & Memory boards		
	. h/w	IAC	20'
	. s/w functionality	IAC/SAp	20'
10.50	Coffee break.		
	- DRCU	SAp	20'
	- Harness.	SAp	10'
	- Test Units	SAp	10'
	- FTS control electronics	LAS	15'
	- Simulators	SO	20'
12.30	Lunch		
14.00	Test facilities		
	- ESGE (h/w & s/w (RTA))	KK	20'
	- Local test units.	SAp	20'
	- Simulators.	SO	20'
15.00	Integration and Test.		
	- SPIRE AIV	KK	20'
	- WE AIV	JLA/CCa	20'
15.40	Preparation of the PDR.	KK	20'
16.00	End of meeting.		

WE Team Organisation & Work sharing



SAp	**C.Cara**	WE System Design; SPU HL s/w; DRCU; BAU; Harnesses; FPU Simulator; WE Integration
IFSI	**R.Cerulli** **R.Orfei**	DPU h/w; DPU LL & HL s/w, Power Supply Unit
IAC	**J.Herreros**	SPU h/w; SPU LL s/w; Memory boards
LAS	**D.Pouliquen**	FTS Control Electronics
SO	**H-G Floren**	DRCU Simulator
RAL	**T.Dimbylow**	RTA/QLA

WE Meetings

WEG meetings:

- **Quarterly** (called by the WE Unit Manager).

  Proposal to link this meeting to the quarterly reporting to ESA.

  Held preferentially at SAp (2 out of 3)

- **Attendance: WE Unit Manager, WE System Responsible,**
  WE Contact points.
  As required: SPIRE PM, SYSTEM Engineer,
  Other WEG members.

- **Addressed Subjects: Managerial, QA, WE System** (design & Interfaces)
  Specific discussions (if any).

Specific WE meetings:

- **Called on demand by the WE Unit Manager.**

  Held at one of the WEG institutes as circumstance require.

- **Attendance: Depends on addressed topics.**
- **Aim: sorting out of specific points.**

Reporting

Ref: [1] e-mail K.King – 20/1/99
[2] Fax ESA - PT-06175 – T.Passvogel – 16/12/98
[3] Fax ESA - PT-06172 – P.Estaria – 16/12/99

- Monthly and Quarterly reports requested by ESA.
- Instrument development report:

  - Template proposed by ESA [2], by SPIRE (KK) [1].

  - Local Managers report to Unit Managers who report to the Project Manager (K.King) who in turn reports to ESA.

  - The WE Unit Manager (SAp) collects report from IFSI, IAC, LAS, SO & SAp

Problem:

- given the lack of Workplan and Schedule, present reports can only reflect the activities and not the progress (i.e. no monitoring can be performed). Only the Actions can be monitored but their fulfilment do not provide information on progress.
- As long as progress cannot be worthily reported, a monthly reporting basis looks inadequate.

WEG participation to the FIRST/Planck Commonality WGs

CWG Definitions (not yet frozen):

Ref: Fax P.Estaria du 3/11/99 – PT-06033 amended by the Minutes of 11/11/98 meeting: Fax P.Estaria du 12/11/99 – PT-MM-06060

#1 #2 – S/C Interfaces and H/W Simulators
– Microprocessors and Components
– Common part procurement co-ordination

#3 – RTA (QLA removed as judged too Instrument specific)

#4 – O/B Software requirements.
– Instrument Operations
– Definition of an overall test philosophy

#5 – Operations and Test Language (Not started before mid-2000)

#6 – FINDAS and IDIS

WEG participation to CWGs:

CWG #1 #2 : H.Dzitko (SAp), V.Mauguen (SAp), C.Cara (SAp)
R.Orfei (IFSI)*, R.Cerulli (IFSI)*, J.M.Herreros (IAC)*

CWG #3 : T.Dimbylow (RAL), R.Gastaud (SAp)
A. Di Giorgio (IFSI)*

CWG #4 : D.Pike (RAL), J-L.Auguères (SAp)
R.Cerulli (IFSI)*

(*): Cross Instrument Support.

WE Documents

Input Documents:

Documents	Comments
Instrument Interface Document - Part B.	The last version (V 0-1 dated 28/2/99) is far from being complete.
FIRST/Planck OIRD	
System Requirement Document	Shall cover the Scientific Requirements (Preliminary version available only)
FPU specification document	WE/ FPU Interface description.
SPIRE Development Plan including development Schedule	Not issued yet (preliminary draft handed out)
SPIRE AIV Plan	
SPIRE Product Tree	Not yet complete
SPIRE Product Assurance Plan	Preliminary draft available.

WE Reference Documents (to be written at WEG level):

Documents	Comments
WE Requirement Document	TBW For both h/w & s/w
WE Architecture Document	TBW
WE Development Plan	TBW
WE Unit ICDs	TBW
WE I&T Plan	TBW

Current Issues

These issues are deeply hampering the WE definition progress.

- **Lack of agreed overall schedule.**
- **Lack of agreed Development Plan.**
- **Scientific and System requirements not yet defined.**

  In particular, fundamental system parameters still open.
- **Ongoing Detector selection process (till Jan. 2000).**
- **Confusing situation regarding the Model definitions:**
  - With ESA: EM & EQM still mentioned in the SPIRE IID-B
  - Within the SPIRE Consortium (development plan).

  As a consequence: no reliable definition concerning AVM, CQM and FS.

Action review

WEG Actions

- **SAp/IAC meeting - IAC - Nov. 16, 1998**

Action 1	IAC/JH		Open	Draft an SPU Development Plan

- **Warm electronics & S/W working group splinter meeting (SPIRE Consortium Meeting - RAL - Dec. 1-2, 1998)**

Action 1	SAp/CCa	08/12/98	Closed	Make a fair copy of the essential input list and send it to Bruce (copy to the WE&SW Group)
Action 2	BMS	20/01/99	Open	To respond the essential input request list.
Action 3	KJK	15/12/99	Open	To provide a Development Plan containing AIV information as well..
Action 4	SAP/LR	15/01/99	Open	To draft a skeleton of the electronics specifications with the electronics requirements identified so far.
Action 5	SAP	05/01/99	Closed	To propose a date and a draft agenda for the next WE&SWG meeting.

- **SAp/IFSI meeting - IFSI - Feb. 16, 1999**

Action 1	KJK	asap	Open	To provide asap a reasonably stable version of the SPIRE development plan (including schedule and a flow diagram).
Action 2	IFSI & SAp	15/03/99	Open	Comment the preliminary draft of the SPIRE Development Plan.
Action 3	SAp/JLA	15/03/99	Closed	To issue a draft agenda for the next WEG meeting.
Action 4	SAp/JLA	10/03/99	Closed	To issue the first draft of the note on the DPU/SPU vs. DPU alone choice.
Action 5	IFSI & SAp	03/03/99	Closed	To raise the DSP vs. SPARC issue at the March 3 CWG #2 meeting.
Action 6	IFSI & SAp	03/03/99	Closed	To raise the DMA issue at the March 3 CWG #2 meeting

Action review

WEG related CWG Actions

- **CWG #4 - Feb. 10, 1999**

Action 3		20/05/99	Open	SPIRE to confirm allocation of responsibilities for SPU h/w & s/w implementation.
Action 5		06/05/99	Open	Generate and Co-ordinate "requirements" on instrument commanding.
Action 7		06/05/99	Open	Define OBSW related milestones and activities till end 99.
Action 8		06/05/99	Open	Provide comments to Appendix 1 of Mission Operation Scenario.

- **CWG #3 - Feb. 3, 1999**

Action 3		19/05/99	Open	Provide plans for ILTs, indicating required deliveries (S/C simulator, CCE,...)
Action 8		30/04/99	Open	Comment on PACS RTA requirements used for SCOS testing.
Action 9	RAL	05/03/99	Open	To supply estimates of manpower available for RTA related activities.

- **CWG #1 #2 - March 3, 1999**

Action 1		25/05/99	Open	Submit list of needed common parts.

Status of the SAp

SAp involvement in the Instrument development:

Electronics:

- **Integrate & Deliver the integrated warm electronics.**
- **Co-ordinate the developments of h/w and s/w WE electronics subsystems. (both managerial & system aspects).**
- **Develop the DRCU except the FTS electronics control system.**
- **Develop the SPU O/B s/w.**
- **Develop the BAU (if CEA's detectors selected).**
- **Develop the Warm harness.**
- **Develop the WE local test unit (h/w & s/w). (In collaboration with the SIG).**
- **Develop the FPU simulator. (In collaboration with the SIG).**

Detectors (in collaboration with the CEA/LETI):

- **Develop (LETI), test, characterize and provide the detector focal planes (if CEA's detectors selected).**
- **Carry out the necessary radiation qualifications.**

He3 cooling system (CEA/SBT development):

- **Provision of the He3 cooler.**

The present team:

Laurent Vigroux	Co-PI
Louis Rodriguez	System Responsible
Jean-Louis Auguères	Project Manager at SAp
Christophe Cara	WE System Electronics Responsible

Quality Assurance

Françoise Loubère

Detector Development & Tests

Louis Rodriguez	Responsible
Yann Le Pennec	
Jerôme Martignac	

Electronics

Christophe Cara	Responsible
André Bouère	
Eric Doumayrou	
Michel Lorgeou	

Mechanics & Thermic

Thierry Tourette

Project Milestones
(still not agreed)

PDR A	07/1999	Optics, Cryogeny, Structure
Final Detector Delivery	09/1999	to QMW
PDR B	09/1999	Electronics
ITT	10/1999	S/C Invitation to Tender
DAS	01/2000	Detector Array Selection
CDR	04/2000	SPIRE Critical Design Review
IPC	10/2000	
Start Phase B	01/2001	
SRR	07/2001	System Requirement Review
SDR	07/2002	System Design Review
Start Phases C/D	07/2002	
AVM Delivery	04/2003	Avionic Model (former EM)
CQM Delivery	04/2003	Cryogenic Qualification Model
CDR	10/2003	Critical Design Review
PFM Delivery	07/2004	Proto Flight Model
QTR	10/2004	
FS & Subassemblies	07/2005	Flight Sparc delivery
FAR	09/2006	Flight Acceptance Review
FRR	03/2007	Flight Readiness Review
Launch	04/2007	

Model Definition (1)

Ref: Preliminary Draft of the SPIRE IDP (v0.1 - 16/2/99)

BBM : Not deliverable to ESA

Availability: TBD

Test Unit	DPU	SPU	DRCU	BAU	FPU Sim
X	X	X	X	X	X

Built with commercial parts. No constraint on physical dimension. No redundancy.

- Unit Interface verification.
- O/B S/W tests.
- RTA/QLA interface verification.
- Validation of AIV procedure.
- Partial EMC test (TBC)

Model Definition (2)

AVM electronics : Deliverable to ESA

Availability: TBD

Test Unit	DPU	SPU	DRCU	BAU	FPU Sim
	X	X	X	?	X

Qualified parts (TBC). Redundancy not fully implemented.

- S/C - SPIRE WE Interface verification.
- Verification of the instrument autonomy functions.
- Validation of O/B S/W Updates.
- Validation of AIV procedure.
- EMC tests
- Thermal Vacuum Test.
- Warm Vibration.
- **Used as CQM electronics.**

CQM electronics: Deliverable to ESA

Availability: TBD

Test Unit	DPU	SPU	DRCU	BAU	FPU Sim
	X	X	X	X	

Qualified parts (TBC). Redundancy fully implemented.

Use of AVM electronics.

Goal:

- Verification of the compatibility with the Payload and S/C.

Model Definition (3)

PFM electronics : Deliverable to ESA

Availability: TBD

Test Unit	DPU	SPU	DRCU	BAU	FPU Sim
	X	X	X	X	

Qualified parts. Redundancy not fully implemented.

- S/C Integration
- Undergoing of qualification tests.

FS electronics : Deliverable to ESA

Availability: TBD

Test Unit	DPU	SPU	DRCU	BAU	FPU Sim
	X	X	X	X	

Qualified parts.

Flight Spare replacement policy not yet agreed: Full model or Spare units.

Products & Tests vs. Models (1)

		Resp.	BBM	AVM	CQM	PFM	FS	Comments
WE UNITs								
DPU								
	Electronics							
	CPU Board	IFSI	1	2	2	2	1	
	Memory	IFSI	1	2	2	2	1	
	Power Supply	IFSI	1	2	2	2	1	
	Component Grade		Std	Mil	Mil	Qual	Qual	
	Mechanics							
	DPU Box	IFSI	1	2	2	2	1	
	Connectors	IFSI	X	X	X	X	X	
	S/W							
	LL s/w	IFSI	V0	V1	V1	V flight	V flight	
	HL s/w	IFSI	V0	V1	V1	V flight	V flight	
SPU								
	H/W							
	CPU Board	IAC	1?	2?	2?	2?		
	Memory	IAC	xMo	2*(xMo)	2*(xMo)	2*(xMo)	xMo	
	Power Supply	IAC	1?	2?	2?	2?	1	
	Component Grade		Std	Mil	Mil	Qual	Qual	
	Mechanics							
	SPU Box	IAC	1?	2?	2?	2?	1	
	Connectors	IAC	X	X	X	X	X	
	S/W							
	LL s/w	IAC	V0?	V1?	V1?	V flight	V flight	
	HL s/w	SAp	V0?	V1?	V1?	V flight	V flight	
DRCU								
	Electronics							
	Detector Readout	SAp	X	2?	2	2	1?	
	FTS Control	LAS	X	2?	2	2	1?	
	Cryo Control	SAp	X	2?	2	2	1?	
	Chopper Control	SAp	X	2?	2	2	1?	
	Calib. Source Control	SAp	X	2?	2	2	1?	
	H/K readout	SAp	X	2?	2	2	1?	
	Component Grade		Std	Mil	Mil	Qual	Qual	
	Mechanics							
	DRCU Box	SAp	1	2	2	2	1	
	Connectors	SAp	X	X	X	X	X	
BAU								
	Electronics							
	Buffers	SAp	1		1	1	1	
	Temp. Regulation	SAp	1		1	1	1	
	Component Grade		Std		Mil	Qual	Qual	
	Mechanics							
	BAU Box	SAp	1	2	2	2	1	
	Connectors	SAp	X	X	X	X	X	
Harness								
	DPU to SPU	SAp	1?	1/2?	2	2	1	
	SPU to DRCU	SAp	1?	1/2?	2	2	1	
	DRCU to BAU	SAp	1	1/2?	2	2	1	

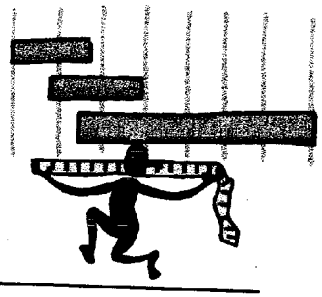
Products & Tests vs. Models (2)

		Resp.	BBM	AVM	CQM	PFM	FS	Comments
Simulators								
FPU Simulator								Developed by CEA/SIG
	Electronics	SAp	1?	1?				
	Mechanics	SAp	1?	1?				
DRCU Simulator								
	H/W							
	Station	SO		1				
	Elect. Interface	SO		1				
	S/W							
	Simulation S/W	SO		1				
Test Facilities								
EGSE								
	Station							
	Elect. Interface							
Local Test Unit								Developed by CEA/SIG
	Station							
	Elect. Interface							
Test Facility S/W								
	OBDH Interface Emulation	SIG						Local Test Unit
	RTA Common	RAL						
	RTA Specific	RAL						
	QLA	RAL						
Tests								
	EMC							
	Thermal Vaccum							
	Vibration							

Criteria	DPU+SPU	DPU alone	Comments
Theoretical O/B CPU power	2 CPU	1 CPU	
Memory needs	Nominal	No global reduction expected	
Board design	DPU and SPU are independent.	DPU shall support all the needed SPU functionality memory. Specific interfaces (TBC) could have to be implemented.	DMA channels are required in both cases.
Power supply	SPU power supply needed	No SPU power supply	The DPU shall supply the needed memory board
Power budget	Nominal	Reduced	SPU board are no more to be supplied.
Mass budget	Nominal	Reduced: by 2 SPU boards to 2 SPU board + an electronic cardcage.	Depends on the still open various options for the electronics implantation.
WE electronics size	Nominal	Globally reduced	Depends on the still open various options for the electronics implantation.
Redundancy	Redundant DPUs and SPUs	Redundant DPU	See attached diagrams.
DPU/SPU interfaces	H/W + S/W	S/W	
Onboard S/W	DPU & SPU have separated functionality.	The DPU support both DPU & SPU functionality.	
FIRST Instruments Commonality	H/W: the present DPU baseline is that the DPUs are identical (TBC). S/W: differences could be expected (depending on the exact DPU/SPU functionality sharing).	H/W: the DPU design shall support extended memory as well as TBC specific interfaces. S/W: DPU functionality are identical, DPU/SPU pure s/w interface instead of H/W and S/W.	
AIV	DPU/SPU integration deal with both h/w and s/w	DPU/SPU pure s/w integration. WE AIV simplified.	
Test facility needs	Nominal	Almost identical	
Reliability	Nominal	Improved	Based only on less h/w consideration.
Development workload	Nominal	Design of an unique board, Simplified integration and documentation writing	
Cost	Nominal	Reduced: depends on h/w amount and workload	See the Pro & Cons section for details.

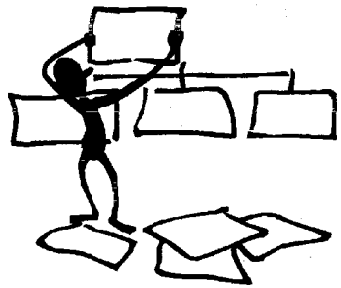
General

- Project Management support
- Quality programme building
- Quality programme implementation
  - Design
  - Manufacturing
  - Assembly and tests
  - Delivery

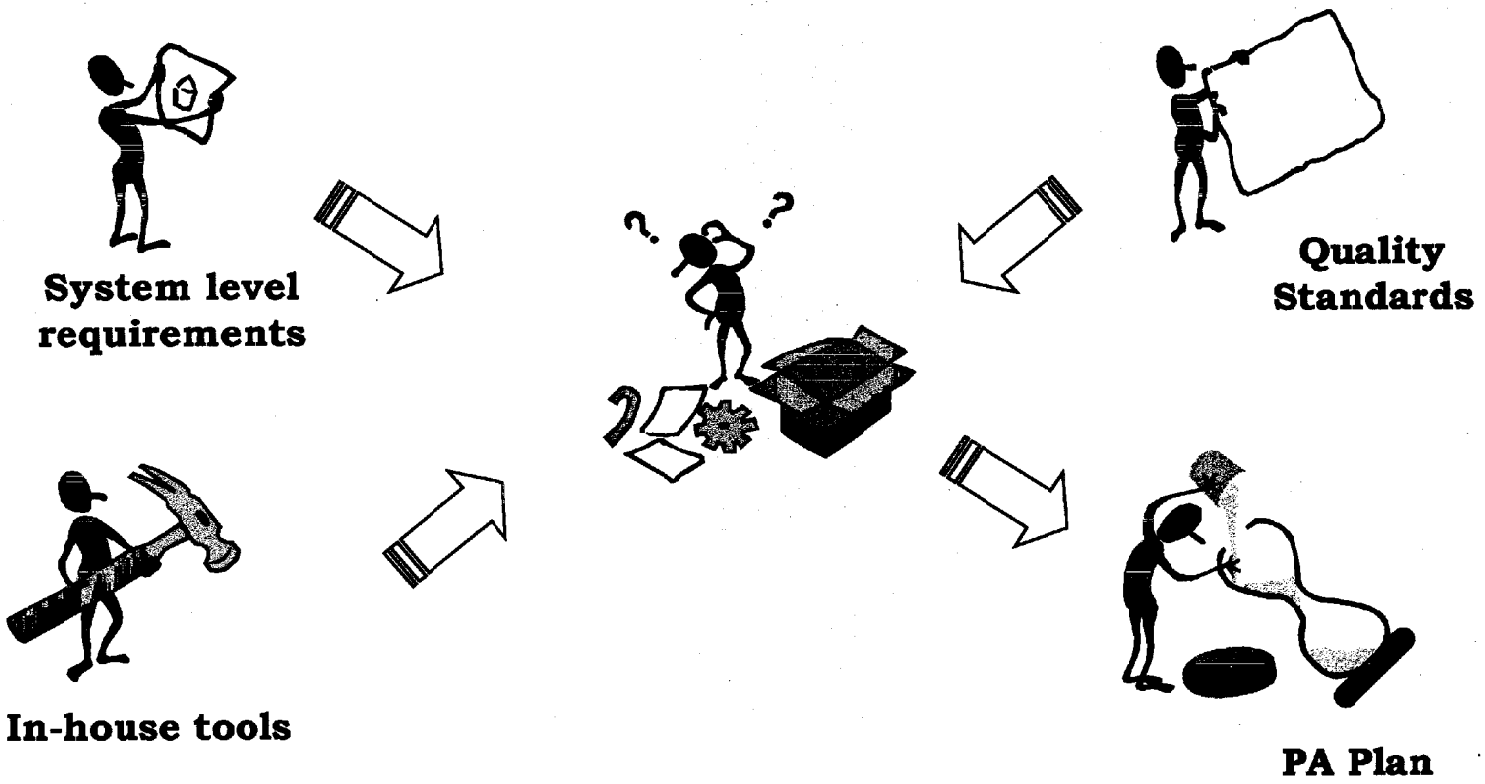


Project Management support

- **Organisation**
- **Validation**
  - **Management plan**
  - **Development plan**
  - **Documentation plan**
  - **Tests plans**
- **Certificate of conformance**
  - **Co-issued with PM**



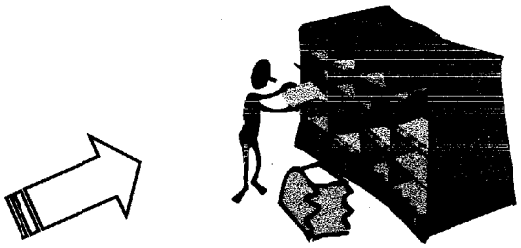
QA programme building



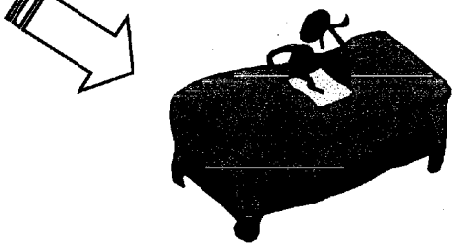
SPIRE

QA programme building

PA Plan



In house organisation and tasks



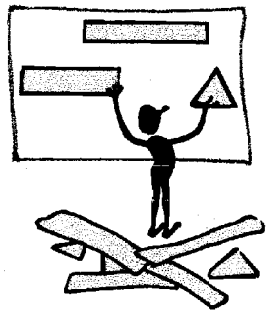
Sub-system level requirements

PA Specification

QA programme building

Definition of :

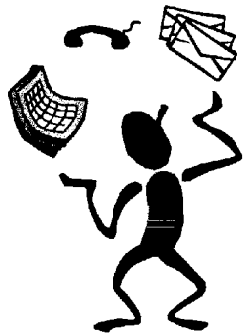
- PA Organisation
- Documentation
  - to be issued and to be delivered
- Configuration control system
  - NCRs, waivers, modifications



QA programme implementation

Permanent actions

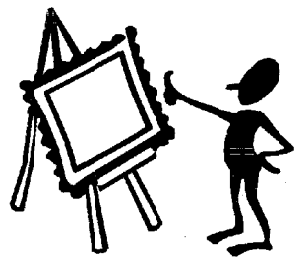
- Relationship with upper system level
- Relationship with sub system level
- Configuration status control
- Procurement sources monitoring
- Evaluation by audits



QA programme implementation

Design phase

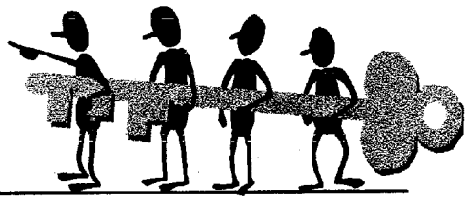
- Functionnal analysis formalisation
- Reliability evaluations
- Parts, Process and materials selection
- Electronic part type reduction, quality level definition, procurement
- Proper design methods selection
  - Software : PSS -05-0 « light »



QA programme implementation

Manufacturing phase

- Design and manufacturing folders verification
- Mandatory key point before launching any realisation and during manufacturing process
  - parts, bare PCBs, wired PCBs
  - mechanics
  - ... and related documentation



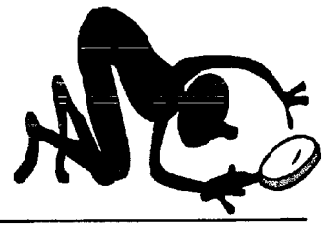
QA programme implementation

Incoming inspections

- parts
- bare PCBs
- wired PCBs
- mechanics

including

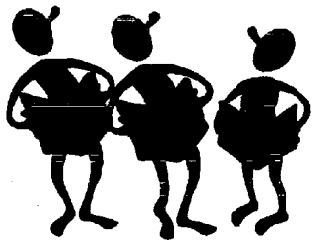
- parts and samples
- visual inspection
- documentation inspection



QA programme implementation

Test phase

- at any stage of development and for any type of test
  - test procedure verification
  - test readiness review organisation
  - test report verification

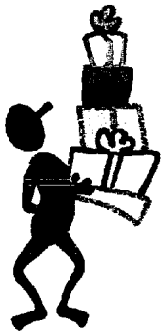


QA programme implementation

Delivery

- Acceptance data package making up and validation

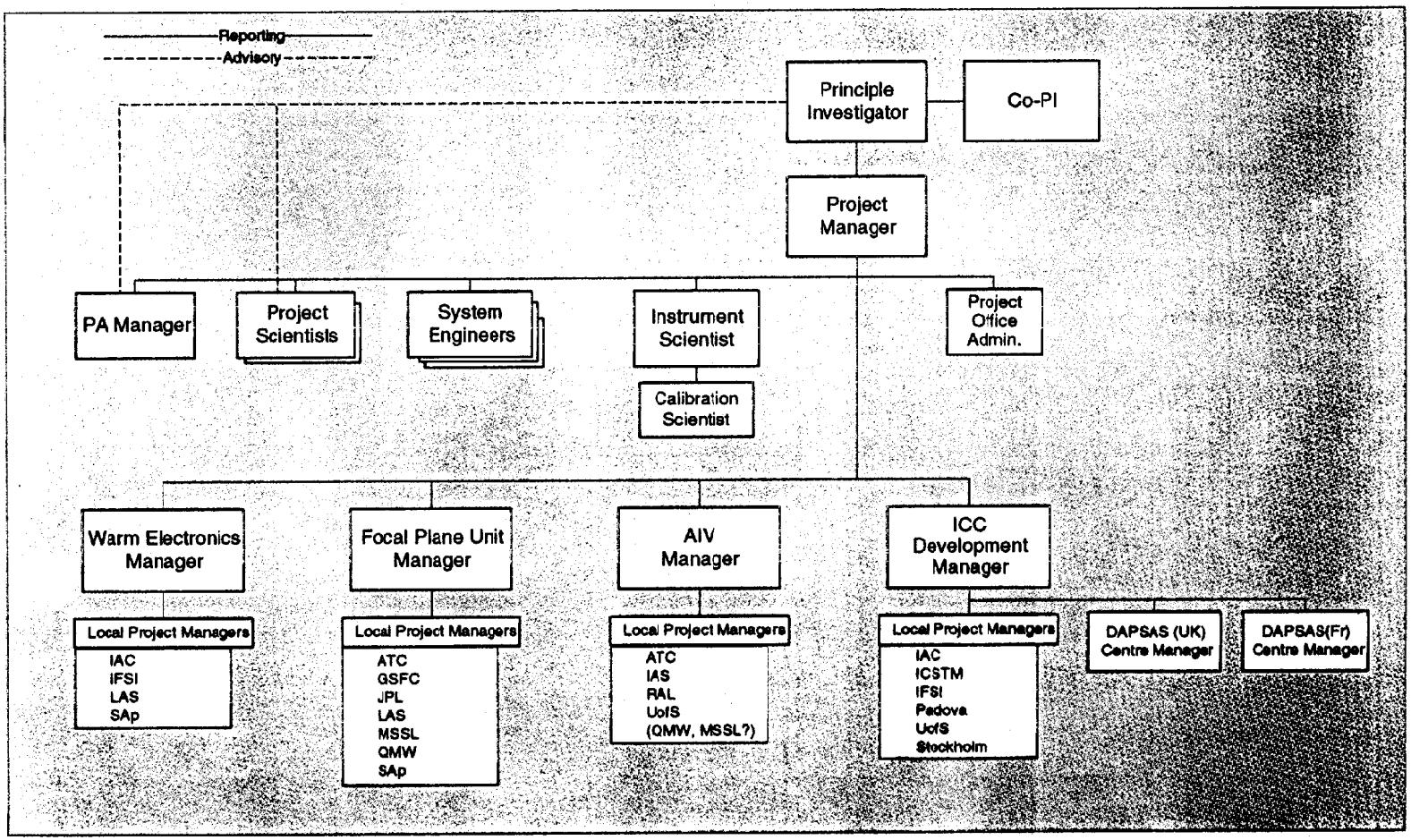
- Mandatory key point before delivery (DRB)

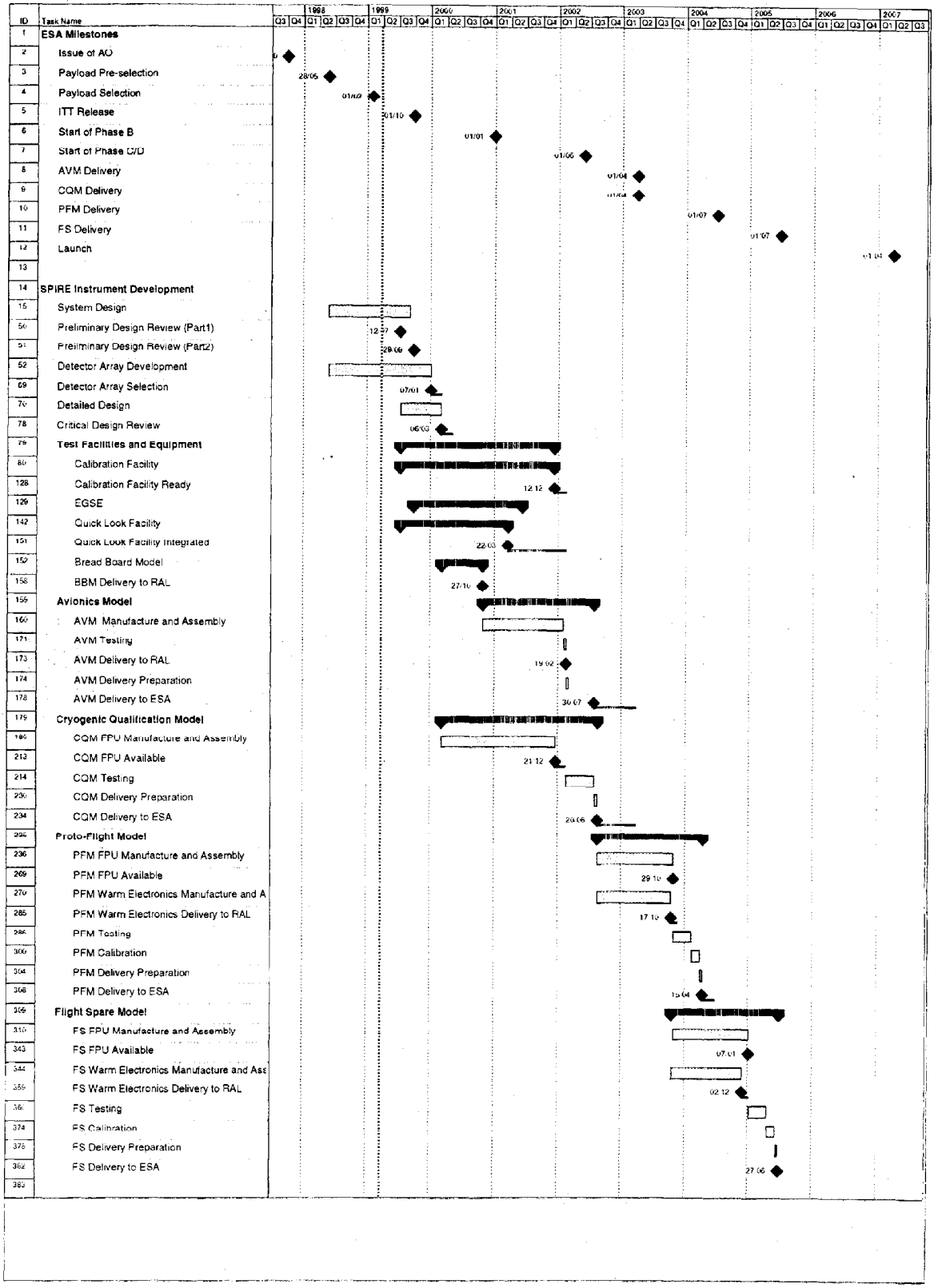


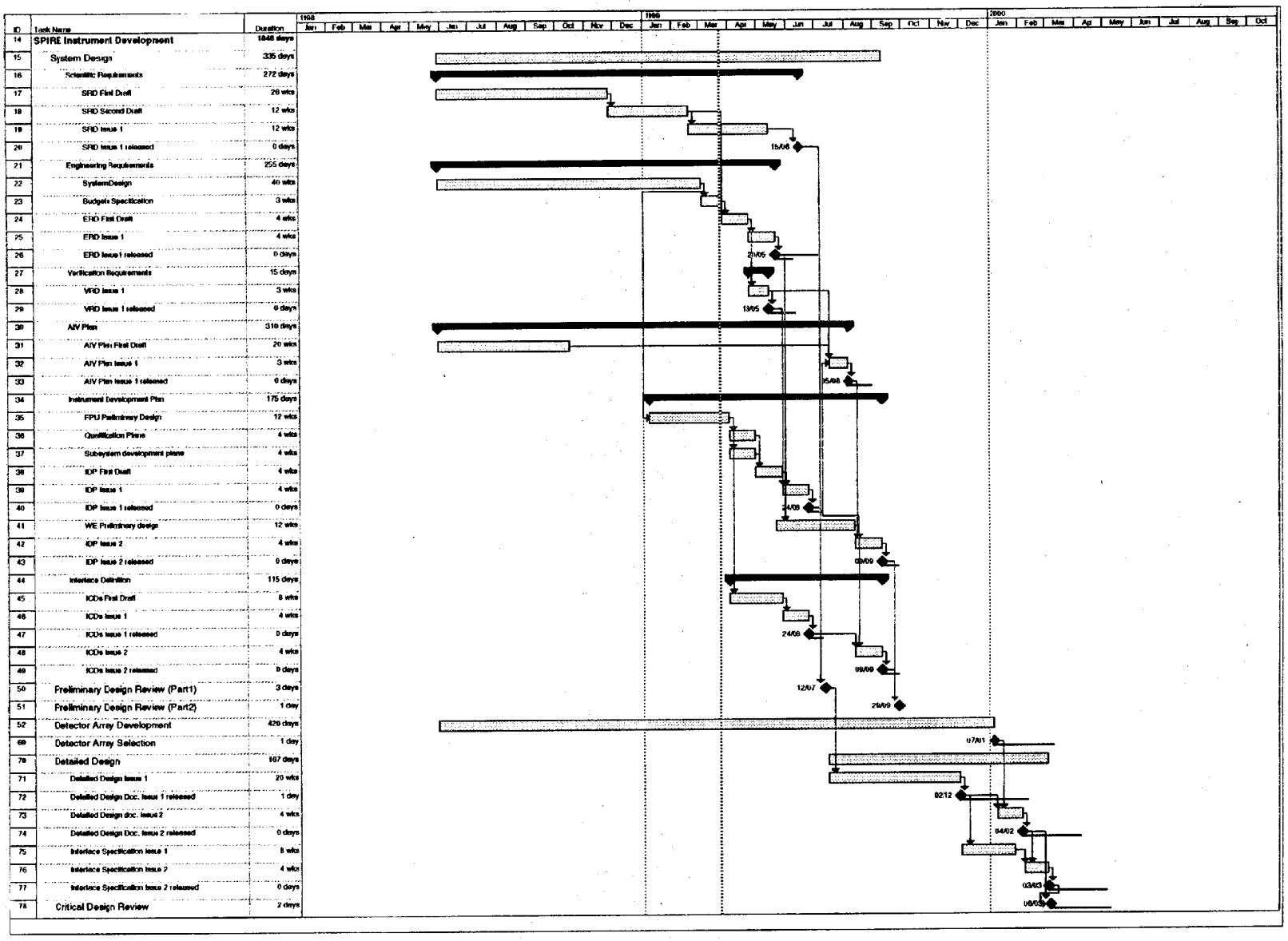
Actions

ACTION	WHO	WHEN
SPIRE Quality requirements issue (trough PA Plan or specification)	RAL	ASAP
List of documents to be produced for PDR	RAL	ASAP
WE PA plan production	CEA (FLo)	04/99
WE sub system Q requirements	CEA (FLo)	05/99
WE sub systems Quality manager designation	institute	ASAP
PA plan production	institute	06/99

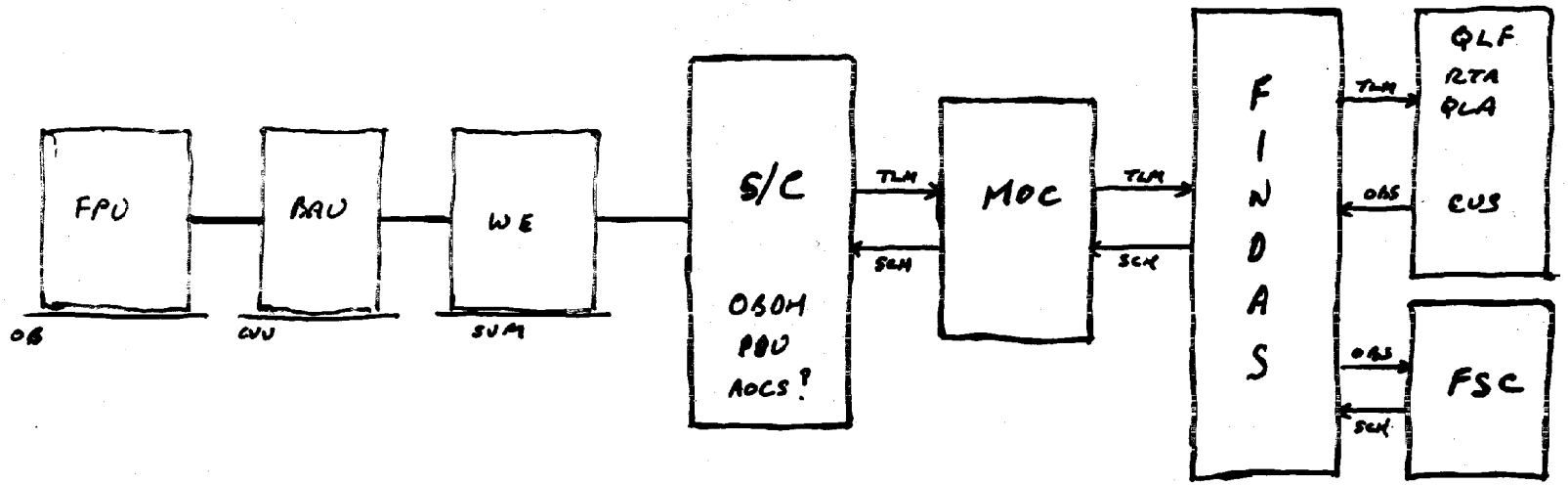
SPIRE Organisation



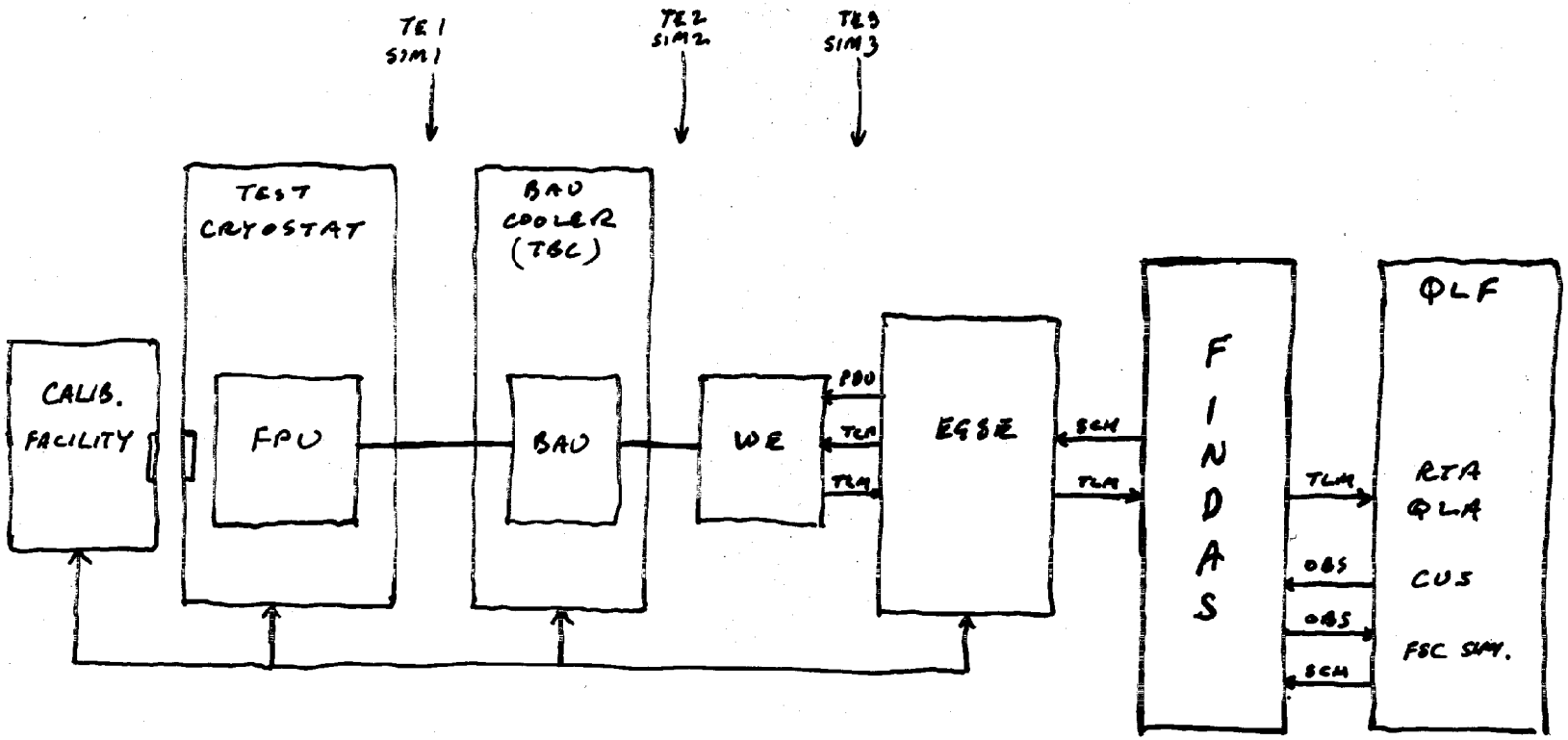

ID
Task Name
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
ESA Milestones
Issue of AO
Payload Pre-selection
28/05
Payload Selection
01/09
ITT Release
01/10
Start of Phase B
01/01
Start of Phase C/D
01/06
AVM Delivery
01/04
CQM Delivery
PFM Delivery
01/07
FS Delivery
01/07
Launch
SPIRE Instrument Development
System Design
Preliminary Design Review (Part1)
12/97
Preliminary Design Review (Part2)
29/06
Detector Array Development
Detector Array Selection
07/01
Detailed Design
Critical Design Review
06/03
Test Facilities and Equipment
Calibration Facility
Calibration Facility Ready
12/12
EGSE
Quick Look Facility
Quick Look Facility Integrated
22/03
Bread Board Model
BBM Delivery to RAL
27/10
Avionics Model
AVM Manufacture and Assembly
AVM Testing
AVM Delivery to RAL
19/02
AVM Delivery Preparation
AVM Delivery to ESA
30/07
Cryogenic Qualification Model
CQM FPU Manufacture and Assembly
CQM FPU Available
21/12
CQM Testing
CQM Delivery Preparation
CQM Delivery to ESA
29/06
Proto-Flight Model
PFM FPU Manufacture and Assembly
PFM FPU Available
29/10
PFM Warm Electronics Manufacture and A
PFM Warm Electronics Delivery to RAL
17/10
PFM Testing
PFM Calibration
PFM Delivery Preparation
PFM Delivery to ESA
15/04
Flight Spare Model
FS FPU Manufacture and Assembly
FS FPU Available
07/01
FS Warm Electronics Manufacture and Ass
FS Warm Electronics Delivery to RAL
02/12
FS Testing
FS Calibration
FS Delivery Preparation
FS Delivery to ESA
27/06



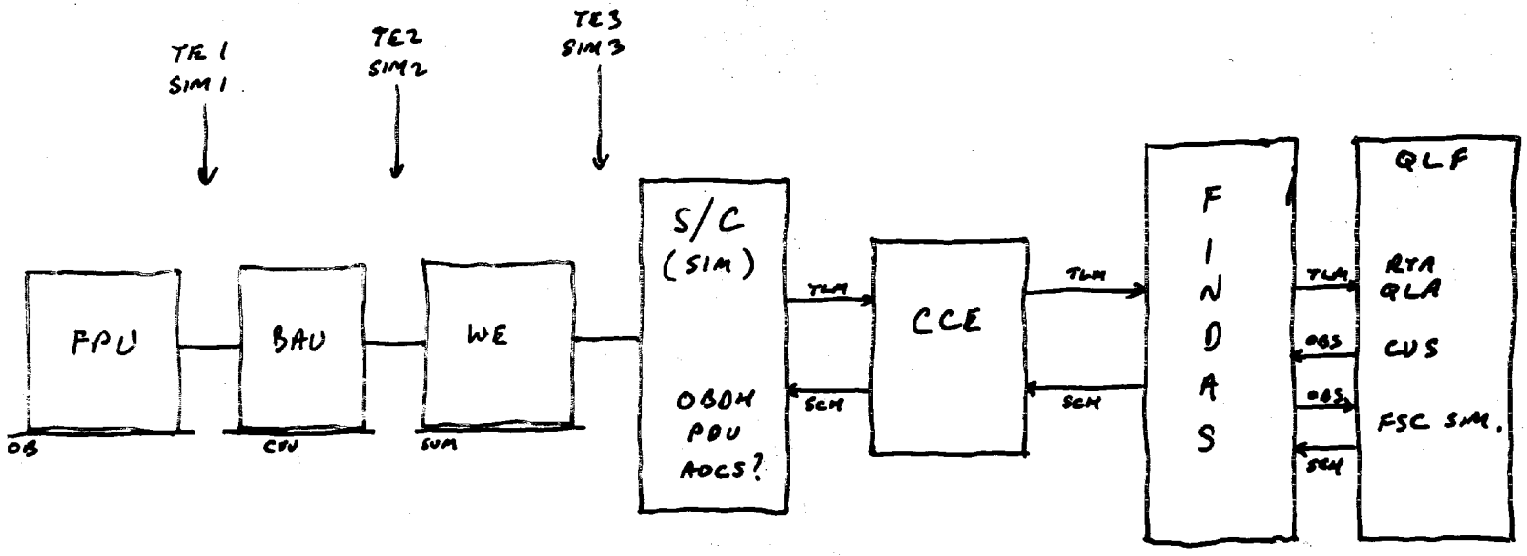
ID	Task Name	Duration
14	SPIRE Instrument Development	1848 days
15	System Design	335 days
16	Scientific Requirements	272 days
17	SRD First Draft	28 wks
18	SRD Second Draft	12 wks
19	SRD Issue 1	12 wks
20	SRD Issue 1 released	0 days
21	Engineering Requirements	255 days
22	SystemDesign	40 wks
23	Budgets Specification	3 wks
24	ERD First Draft	4 wks
25	ERD Issue 1	4 wks
26	ERD Issue 1 released	0 days
27	Verification Requirements	15 days
28	VRD Issue 1	3 wks
29	VRD Issue 1 released	0 days
30	AIV Plan	316 days
31	AIV Plan First Draft	20 wks
32	AIV Plan Issue 1	3 wks
33	AIV Plan Issue 1 released	0 days
34	Instrument Development Plan	175 days
35	FPU Preliminary Design	12 wks
36	Qualification Plans	4 wks
37	Subsystem development plans	4 wks
38	IDP First Draft	4 wks
39	IDP Issue 1	4 wks
40	IDP Issue 1 released	0 days
41	WE Preliminary design	12 wks
42	IDP Issue 2	4 wks
43	IDP Issue 2 released	0 days
44	Interface Definition	115 days
45	ICDs First Draft	8 wks
46	ICDs Issue 1	4 wks
47	ICDs Issue 1 released	0 days
48	ICDs Issue 2	4 wks
49	ICDs Issue 2 released	0 days
50	Preliminary Design Review (Part1)	3 days
51	Preliminary Design Review (Part2)	1 day
52	Detector Array Development	429 days
69	Detector Array Selection	1 day
70	Detailed Design	167 days
71	Detailed Design Issue 1	20 wks
72	Detailed Design Doc. Issue 1 released	1 day
73	Detailed Design doc. Issue 2	4 wks
74	Detailed Design Doc. Issue 2 released	0 days
75	Interface Specification Issue 1	8 wks
76	Interface Specification Issue 2	4 wks
77	Interface Specification Issue 2 released	0 days
78	Critical Design Review	2 days



ROUTINE OPERATIONS SETUP



INSTRUMENT LEVEL TEST SETUP



FIRST SYSTEM LEVEL TEST SETUP

IFSI status report

- **Subsystem Performance.**
  Baseline is still based on the DSP TSC21020E. The ESTEC meeting of CWG #1-2 of March the 3rd has not changed this baseline after various discussions and presentations.

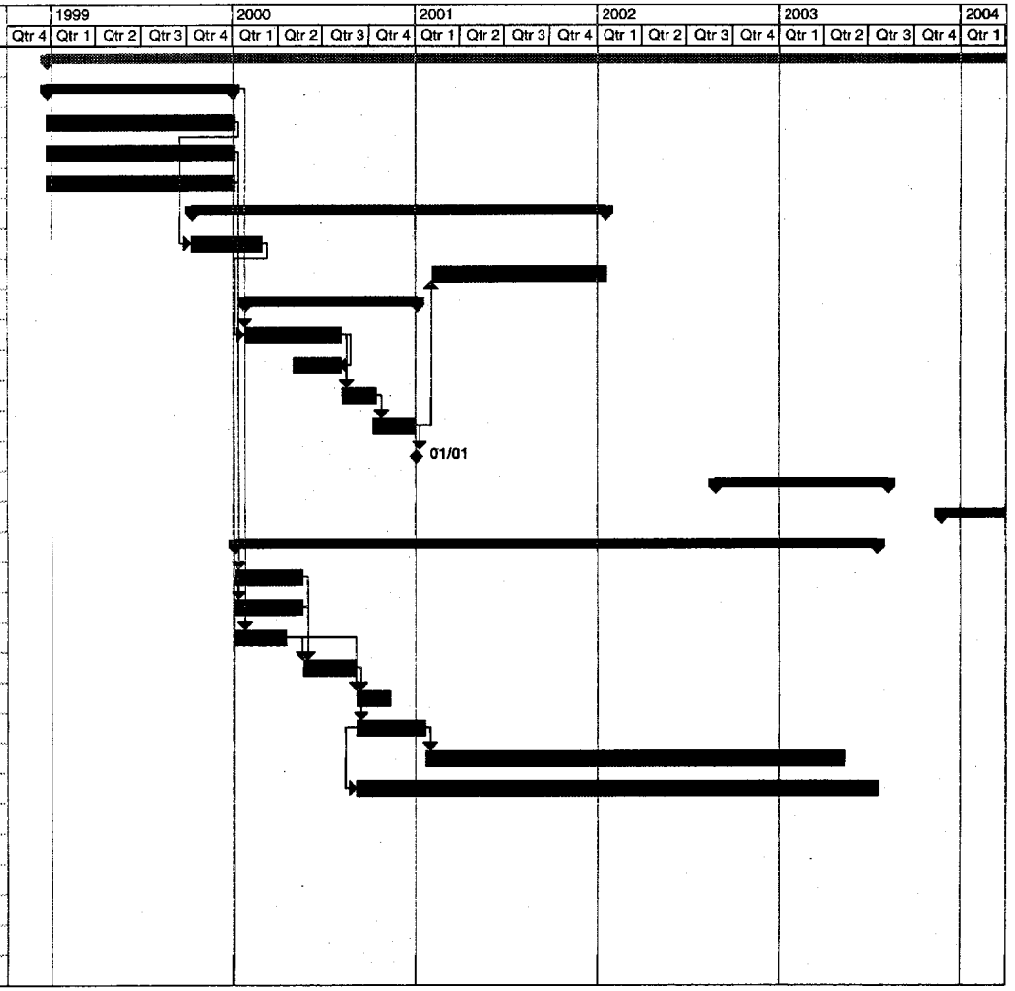
- **Problem Areas and Remedial Action.**
  Instrument - OBDH protocol not yet defined, discussed in the ESTEC CWG #1-2 meeting and likely to be the RBI one.
  The meeting with the Italian Space Agency (ASI) to discuss a contract with industry for procurement of some DPU boards was held on 19th of March and we are progressing on the ITT.

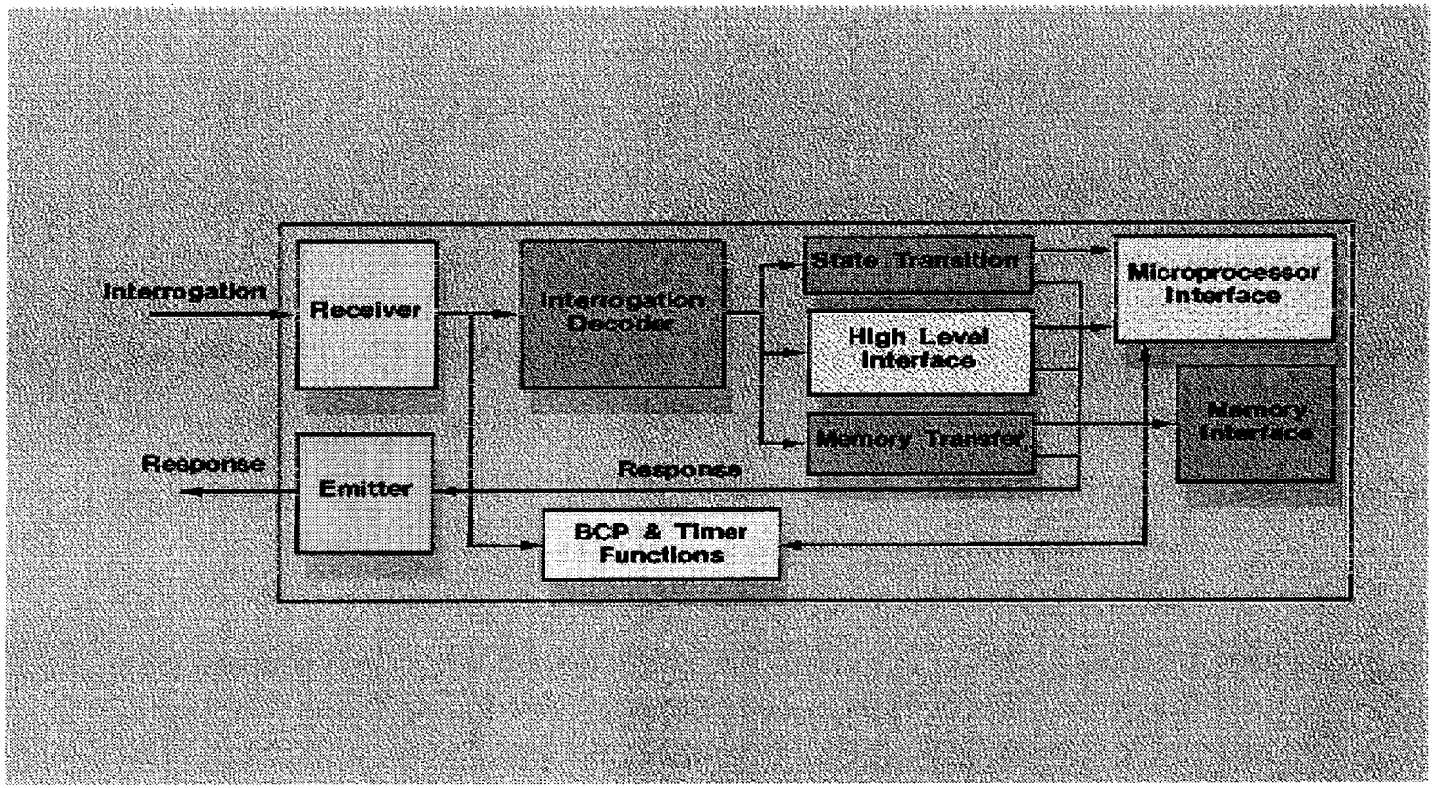
- **Engineering Activities.**
  The low speed bidirectional serial interface bus (proposed by HIFI) has been slightly modified (total length is now 32 bit). Discussions are in progress about the scientific data serial link.

- **Budgets.**
  No information yet of ASI decision about 1999 request for funds (to be mostly used in year 2000), but FIRST is now an established ASI funded programme and this, in principle, should speed-up the funding procedures in the future.

- **Schedule Changes.**
  A new WBS has been sent to the management and accordingly an updated schedule has been prepared.

ID	WBS	Task Name
0	0	**SPIRE_WP**
1	**FS242X400**	**DPU design**
2	FS242X410	Computer design
3	FS242X420	S/C I/F design
4	FS242X430	Subsystems I/F design
5	**FS1A0X100**	**DPU parts procurement**
6	FS1A0X110	Commercial parts
7	FS1A0X120	Hi-Rel parts
8	**FSDPUA100**	**AVM (2 units)**
9	FSDPUA110	Electrical mfg
10	FSDPUA120	Mechanical mfg
11	FSDPUA130	Assembly
12	FSDPUA140	In house tests
13	FSDPUA150	Delivery
14	**FSDPUP100**	**PFM**
20	**FSDPUS100**	**FS**
25	**FSOBSX100**	**OBS**
26	FSOBSX110	S/C I/F module
27	FSOBSX120	Subsys. I/F mod.
28	FSOBSX130	Dedicated OS
29	FSOBSX140	Test mod.
30	FSOBSX150	Health autonomy mod
31	FSOBSX160	AVM issue
32	FSOBSX170	PFM issue
33	FSOBSX180	Documentation





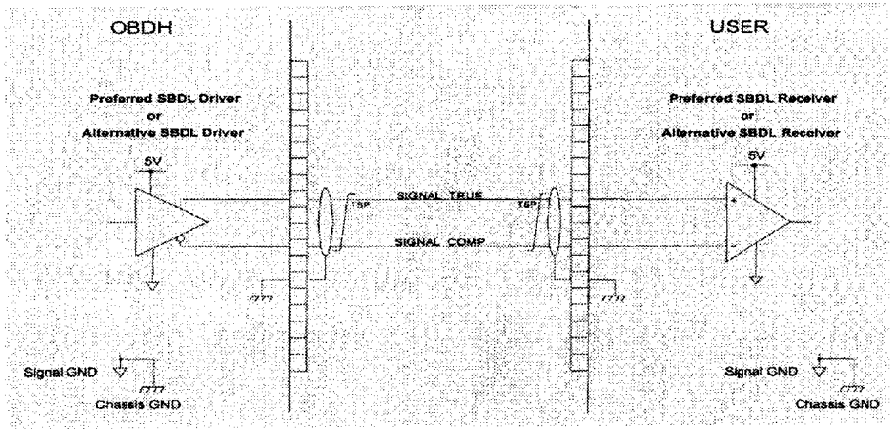
The device is fabricated using MITEL's SOS4 radiation-hard silicon-on sapphire process and encapsulated in a 132-pin package. This choice is justified because the OBDH bus is an essential element of the satellite's command and control chain which must be immune to single-event upset and other space radiation effects.
The RBI chip is manufactured by ADV technologies (MC1031).

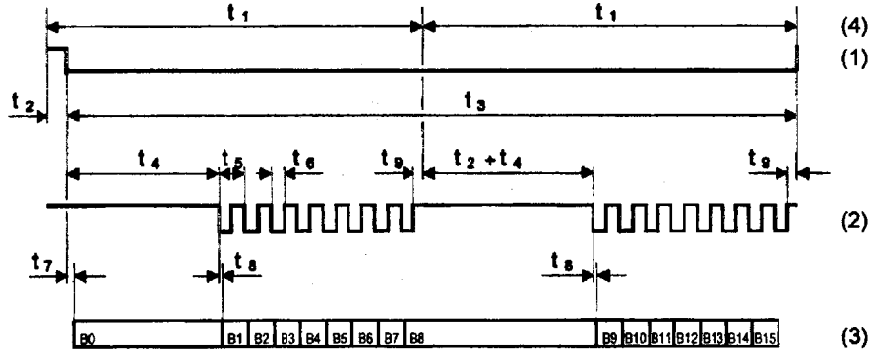
RBI (Remote Bus-Interface).

The standard RBI is an application-specific integrated circuit (ASIC) which implements the OBDH high level protocol and which allows direct transfers of data packets into the memory of the payload computer memory without involving its software. The main benefits accruing from using a standard bus coupler on-a-chip are:

- reduced cost: one common development can be applied to all payloads whose data interfaces all exhibit the same behaviour;
- easy accommodation, small size and low power consumption;
- easy to use since the user need not know the protocol involved.

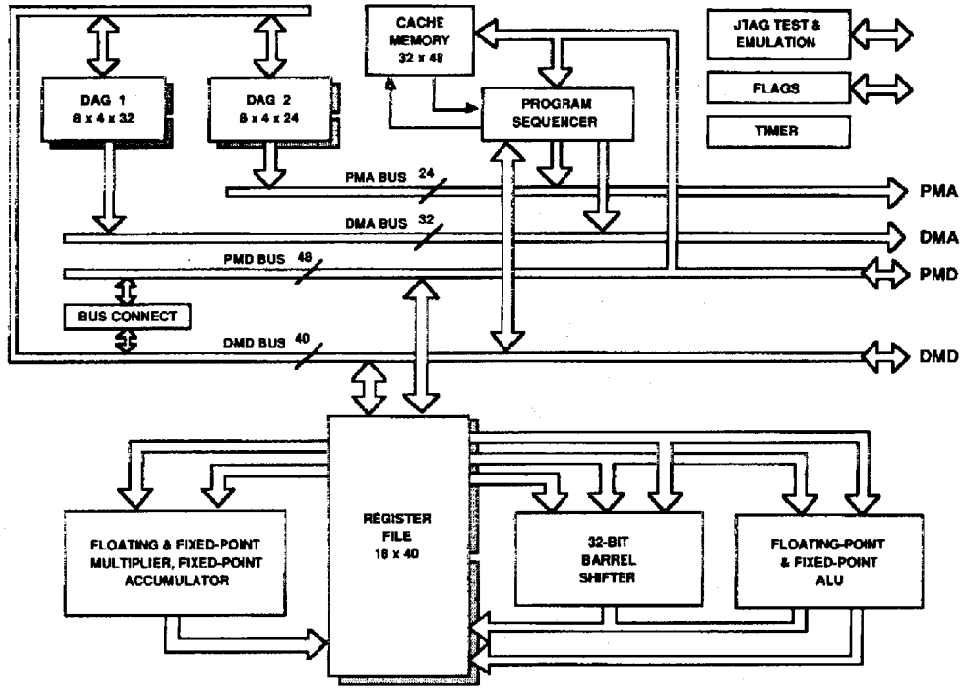
All the above benefits have been demonstrated within the Envisat-1 program, furthermore since the device has now also been adopted by the XMM, Integral and Metop programmes it has become a de-facto standard for ESA satellites.





(1) Sampling signal at the user's input
(2) Serial data transfer clock signal at the user's input
(3) User's serial data at the RTU input
(Bit 0 is transmitted first by the user and is the most significant bit)
(4) Time interval corresponding to the interrogation bus interval

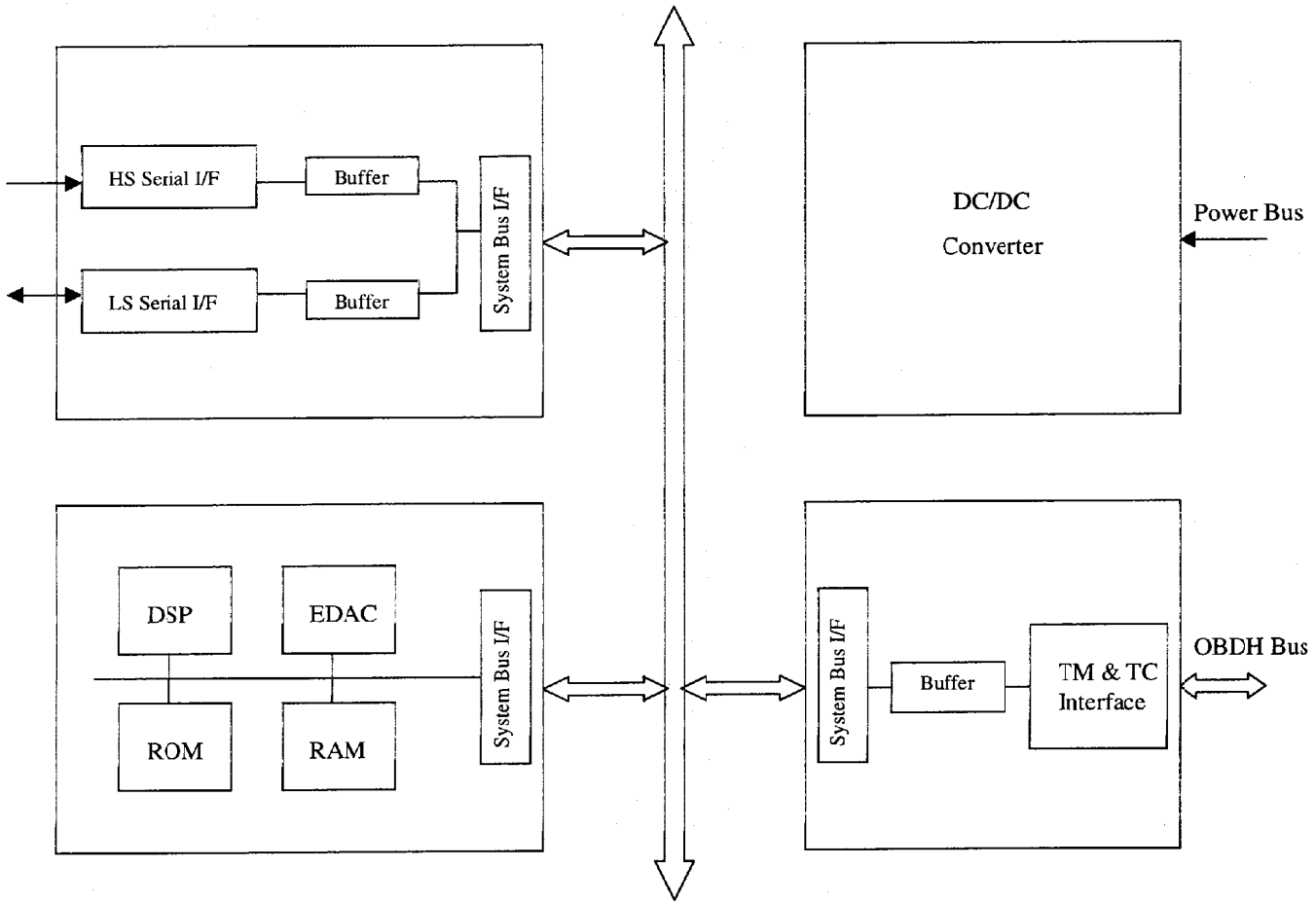
TSC21020E block diagram



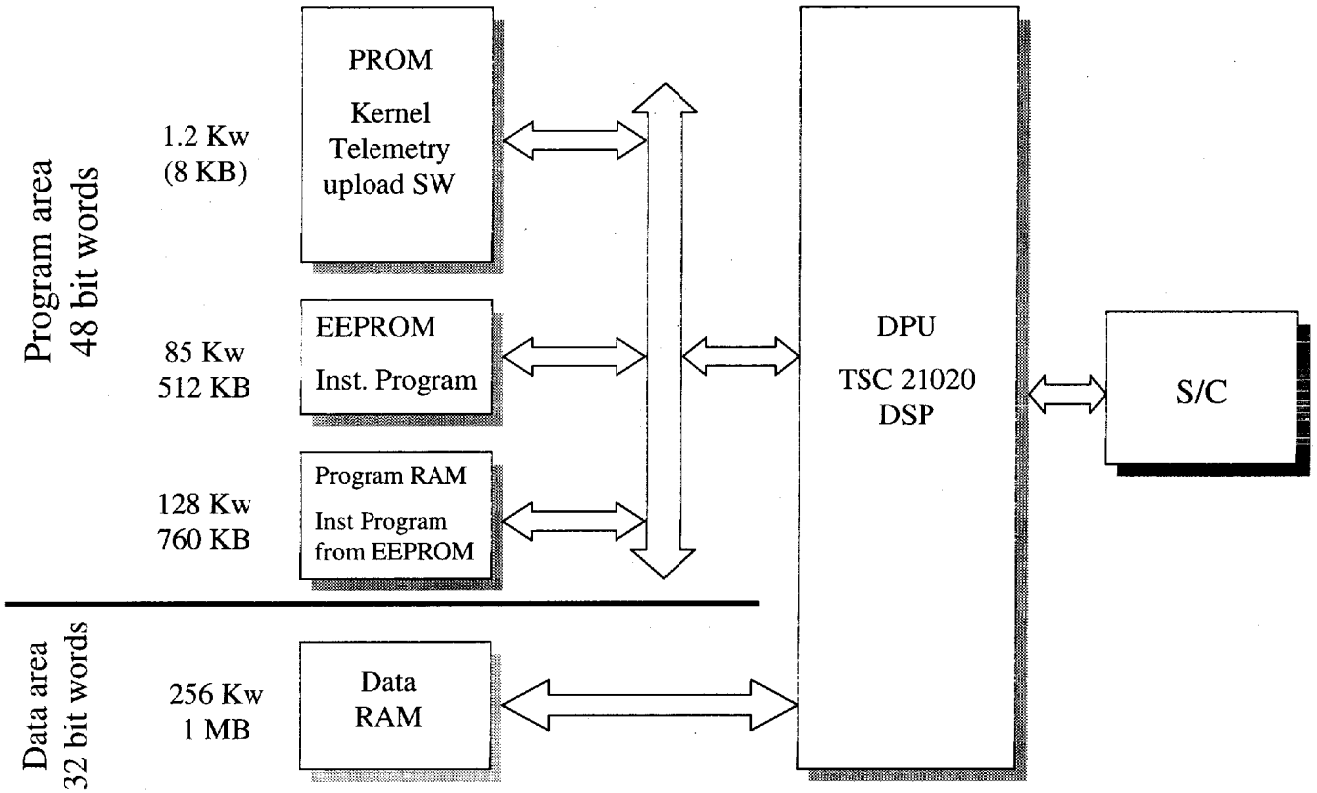
Prog Bus => 48 bit

Data Bus => 32 bit

4 ext. interrupt lines
16 Mw Prog & 4 Gw Data RAM
Internal 32 bit down counter timer


HS Serial I/F
Buffer
LS Serial I/F
Buffer
System Bus I/F
DC/DC
Converter
Power Bus
DSP
EDAC
ROM
RAM
System Bus I/F
System Bus I/F
Buffer
TM & TC
Interface
OBDH Bus

Memory organisation



Interfaces

Present design is based on serial interfaces in order to minimise interconnecting wiring and in agreement with requirements with the other two FIRST instruments. From the noise point of view the reduced number of wires requires a balanced RS-422 interface:

- One high speed data link based on IEEE Std 1355-1995.
- One synchronous serial bidirectional bus. This bus is common for all subsystems and handles commands and HK up to a speed of ~ 100 Kbit/s.

High speed interface

- SPU suggests the use of SMCS 332 .
- This is based on IEEE Std 1355-1995 links (DS-LinkTM):
  3 serial communication links on chip (196 pin CQFP package)
  Up to 200 Mbit/s transfer rate
  Rad tolerant version (50 Krad) available from Temic/MHS
  http://www.omimo.be/new/companies/dasa_001.htm
- Can be a simpler monodirectional synchronous serial I/F (HIFI suggestion)

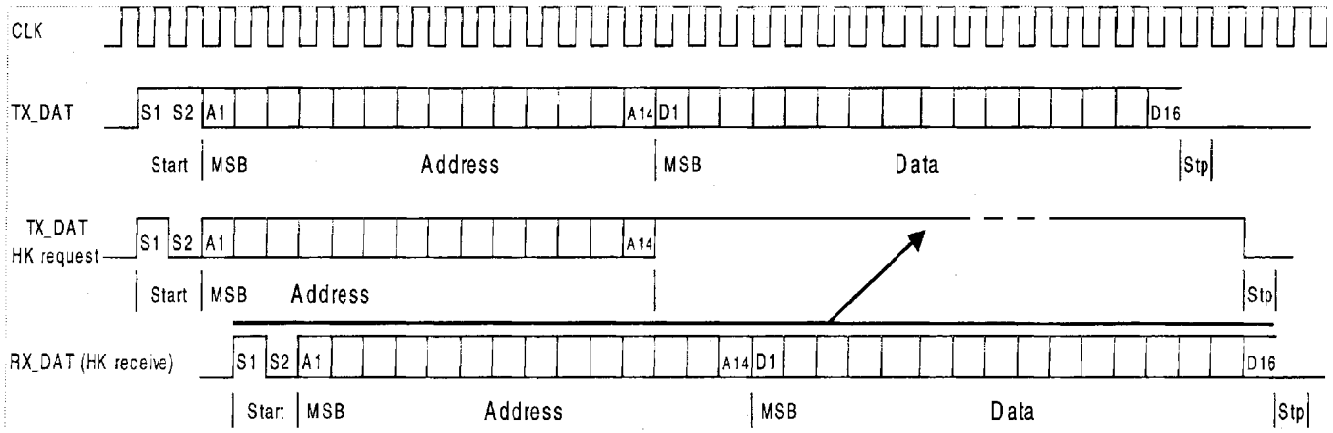
Low speed interface

HIFI proposal adopted and shown.

All data transactions with the addressed subsystem (addr. In TX_DAT), are initiated by DPU.
DPU will send data to all subsystems using one serial data line TX_DAT and can send both commands and HK requests via this line.
Subsystems will send responses via RX_DAT line.

A **command** is made of 2 start bit, 14 address bit, 16 data bit and 1 stop bit.
HK request is made of 2 start bit and 14 address bit. After transmission of these 16 bit, the TX_DAT line shall stay high untill the corresponding HK response has been received. Then 1 stop bit will follow.
A **HK response** shall consist of 2 start bit, 14 address bit, 16 data bit and 1 stop bit

The figure shows the proposed HW protocol. Clock rate ~ 100KHz



Commands

Memory load commands are used to send single instructions to the instrument or to command pre-defined sequences of operations.

A **command** is constituted by a variable number of **telecommand** words: it is formed by the description of the action to be carried-out followed by the definition of the parameters needed for that action.

Each command is formed with a variable number of 16 bit words having the following general structure:

1. a Header describing the Command function;
2. the number of words to follow;
3. the new values of the parameters, if any;

Types of commands

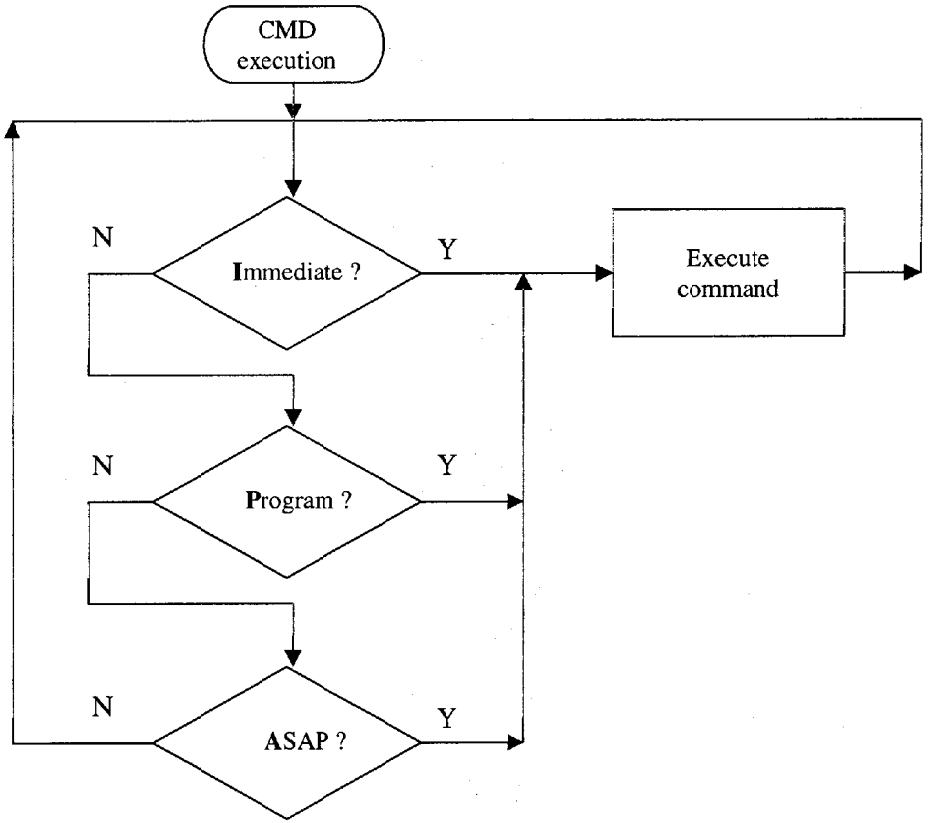
There are two main categories of commands:
- Standard Commands
- Time tagged Commands **T**

The time tagged commands are standard commands that will be executed at a specified time.

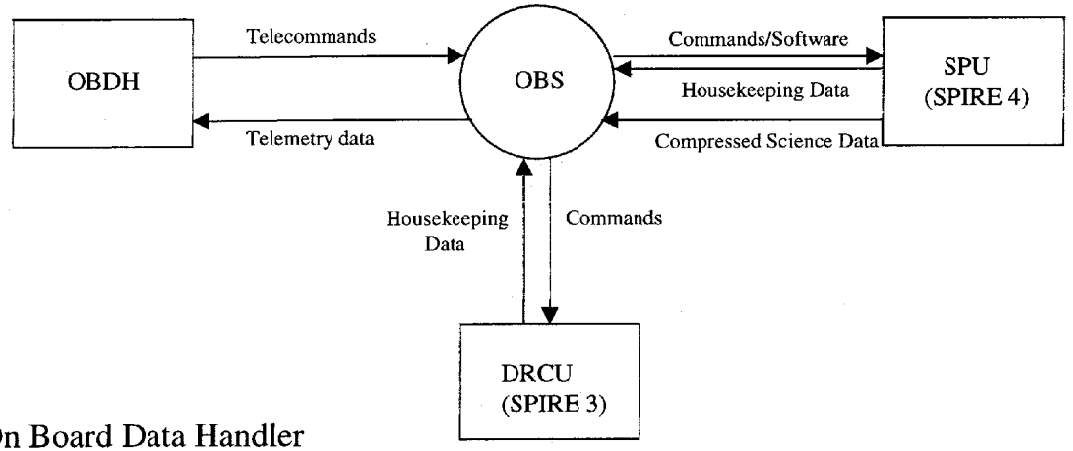
There are 3 types of standard commands, defining the execution priority from high to low, stored in different circular buffers.
- Immediate commands **I**
- Program commands **P**
- ASAP commands **A**

Generally each command can belong to each of the 3 types.
Immediate commands are executed at the end of the current command execution phase.
Program commands, are standard commands executed as a sequence. The sequence (i.e. the program) starts when a **I** or **A** RUN command is executed. A few commands are permitted only as **P** commands (instructions) defining elementary programming language statements (i.e. for loop, if statements, setting of program variables etc).
ASAP commands are executed when no other command type is present.

Commands will range from a simple subsystem parameter change, to a complex macro defining a measurement routine.

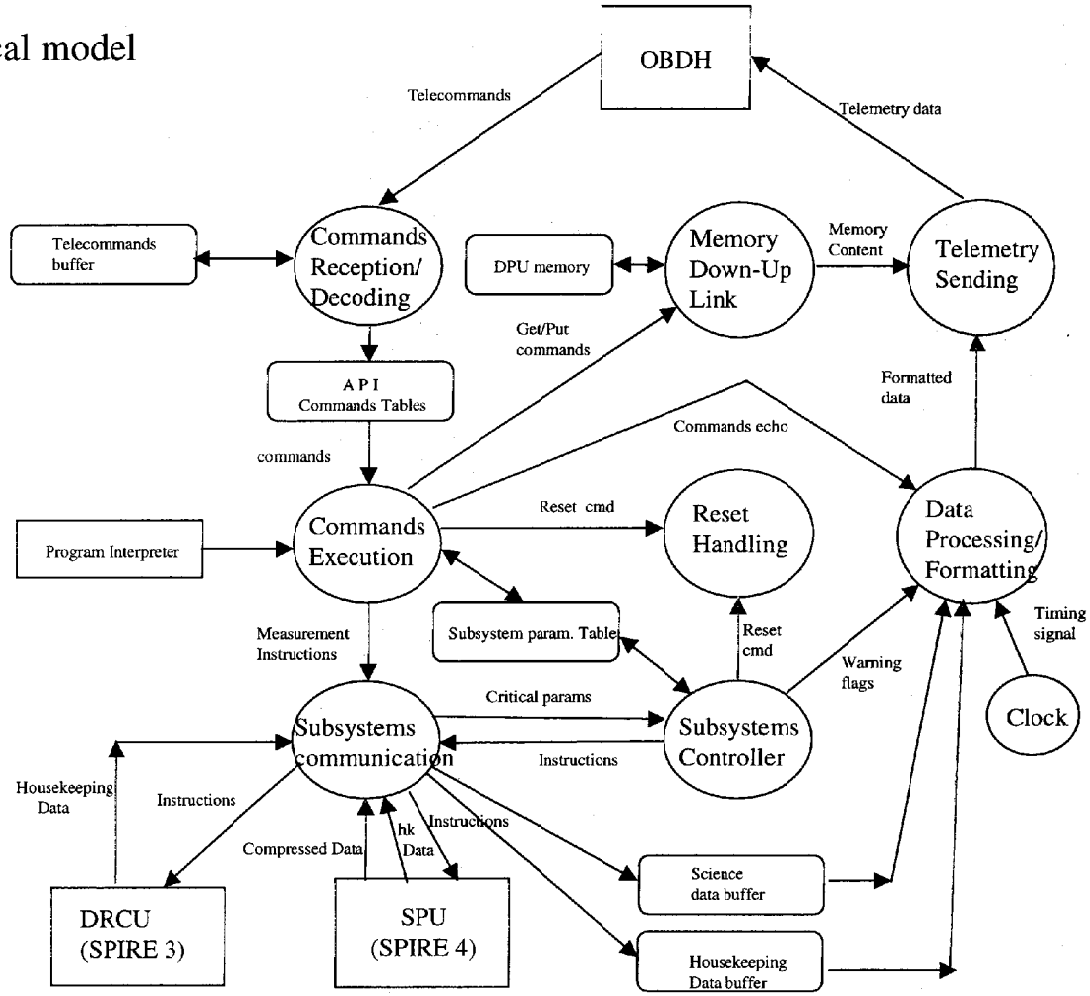

CMD execution
Immediate ?
N
Y
Execute command
Program ?
N
Y
ASAP ?
N
Y

SPIRE On Board Software
Context Diagram



OBDH On Board Data Handler
OBS On Board Software
SPU Signal Processing Unit
DRCU Detector Read-out & Control Unit

SPIRE OBS - Logical model



Functional decomposition

Based on the functional description contained in the SPIRE Scientific and Technical Plan, the following main functional components have been individuated for the SPIRE OBS:

1. Commands Reception/Decoding :

- Receives the telecommands from OBDH and stores them sequentially in the Telecommands Buffer (a cyclic buffer necessary to store all the telecommands as soon as they are received, until they are examined for their decoding and execution);
- Reads the Telecommand buffer, executes a first level analysis, and moves the telecommands to the three Commands Tables (one per execution priority: I, P, A), which contain the received commands sequentially, as they were transmitted.

2. Commands Execution :

- Reads from the Commands Tables the commands to be executed, according to their priority;
- Interprets the Commands according to given algorithms;
- If requested, it passes the RESET command to the *Reset Handling* component;
- Updates the Subsystems Parameters Table(s), which is used for the actual execution of the measurement;
- Sends the relevant sequence of digital commands (Measurement Instructions) to the *Subsystem Communication* component;
- If requested, it passes the memory reading/writing commands to the to the *Memory Down-Up link* component.

Functional decomposition

3. Subsystems Communication:

- It interfaces the instrument subsystems, by sending the measurement instructions, and getting the Housekeeping information from all the subsystems and the compressed science data from the SPU;
- Updates the Science Data Buffer and the Housekeeping Data Buffer;
- Sends the subsystems critical parameters to the *Subsystems Controller* component;
- Receives from the *Subsystems Controller* component the instructions generated after the analysis of the critical parameters and sends them to the subsystems (autonomy functions);
- Sends S/W modules to SPU.

4. Subsystems Controller:

- Receives from the *Subsystems Communication* component the values of the critical parameters;
- Checks the parameters and flags the abnormalities; the warning flags are sent to the *Data Processing/Formatting* component to be included in the Telemetry data;
- In case of autonomous operation, it may take action to switch off parts of the instrument, by sending an appropriate set of instructions to the *Subsystem Communication* component.

SPIRE Warm Electronics & OBS Requirements (1)

Requirements on Warm Electronics and On board Software are driven by :

- **Mission profile :**
  - **mission duration : 4.5 year**
    - **impact on reliability**
    - **impact on detector / mechanism performance**
    - **software uploading**
  - **L2 orbit :**
    - **radiation environment dominated by galactic protons and heavy ions**
      - **total dose ***
      - **SEU rate**
      - **detector ageing / glitches**
    - **48 h autonomous operation**
  - **mission operation :**
    - **telecommands philosophy and engineering mode of operation**
    - **TM and TC maximum rates**

*** FIRST L2 Radiation ESA Document already exists but is probably no applicable to SPIRE W.E.**

→ Instrument Performance :

- spectral range → photometer → spectrometer | Signal processing (detector background level)
- spectral resolution | FTS position measurement /
- sensitivity | Signal processing / AD resolution
- dynamic range |
- field of view | Number of pixels → wiring /electronics complexity/data rate
- spatial resolution |
- scientific mode of operation
- scientific HK (time stampling, FTS position, ...)

SPIRE Warm Electronics & OBS Requirements (3)

→ **Technical constraints :**

- **Detector operation**
  - → **operating temperature**
  - → **signal processing (filtering / demodulation / dynamic biasing / ...)**
- **FTS mechanism operation**
  - → **scan period**
  - → **translation speed**
  - → **position measurement**
- **Chopper mechanism operation**
  - → **scan speed**
  - → **position measurement**
- **Instrument Budgets**

SPIRE Glitches Rejection

ASSUMPTION : only glitches generate "fast transients" signal

• The first "frame" used as reference by the algorithm (just after a start of observation) is uniform. The pixel value given by the pixel's average of the first acquired frame.

• 1st step : the current frame (n) is subtracted with the previous one (n-1) : 1024+576+256 subtractions

• 2nd step : comparison of the pixel differences with a threshold

➔ if the difference is above the threshold (glitched pixel) :
→ pixel value is set to zero
→ the "decay" period (expressed in number of frame) is computed as a function of the glitch amplitude

➔ if the difference is below the threshold (valid pixel) :
→ update of the "number of added frame" table

➔ if the pixel is already identify as a glitched pixel
→ pixel value is set to zero
→ the "decay" period is decremented

• 3rd step : addition of the corrected image (n) with the previous one (n-1)

• 4th step : when N frames are co-added → transfer into the output buffer

SPIRE Acquisition Rates

Photometer

Central Wavelength µm	Theorical array sizes	Practical array sizes	Number of pixel	Acquisition rate rate Hz [1]	Number of acq. /s	Number of bits	Data rate bits/s
250	**32x32**	32x32	1024	40	40960	14	573440
350	**24x24**	32x32	576	40	23040	14	322560
500	**16x16**	16x16	256	40	10240	14	143360
						Total (average) :	1039360

1 : Assuming a 2 time oversampling

Minimum compression factor compared to **40 kbits/s** (200 kbits/s-TBC) : **26** (5) → **Image rate = 1.5 /s**
Real compression factor will take into account data format (i.e. 3 bytes / pixel)

Spectrometer

Wavelength µm	Theorical array sizes	Practical array sizes	Number of pixel	Acquisition rate rate Hz [1]	Number of acq. /s	Number of bits	Data rate bits/s
200-300	**16x16**	16x16	256	40	10240	14	143360
300-600	**12x12**	16x16	144	40	5760	14	80640
						Total (average) :	224000

1 : Assuming a 2 time oversampling

Minimum compression factor compared to **40 kbits/s** (200 kbits/s-TBC) : **6** (1.12 !) → **Interferogram rate = 1 / 240 s**
Real compression factor will take into account data format (i.e. 3 bytes / pixel)

SPIRE Signal Processing Memory Needs

• Dominated by the SPECTROMETER high resolution mode memory requirements (if full spectrum co-addition).

• Assuming a 40 second scanning duration the amount required to store one scan is :

Number of arrays	Number of acq. /s	Quantization in bytes	Memory size in bytes
2	10240+5760	2	1280000

• Total Memory required includes :

- currently acquired spectrum : 2 bytes
- sum of the spectra (6) : 3 bytes
- deglitching table : 1 bytes

Total : 3.84 Mbytes

• Oversampling (factor of 1.5) may be required ➔ Total with margin : 6 Mbytes

➔ Memory could be saved if data reduction is based on error-free data compression algorithm insteed of performing co-additions : no more need for "sum of spectro" & "deglitching" buffers.

SPIRE Autonomy (1)

• Autonomy constraints requires on-board analysis of scientific data or HK to react during instrument operation (IID-B and OIRD).

➔ The instrument shall be able to adjust parameters or/and switch operating mode or/and activate redundancy when an anomaly occurs.

Comment : A Safe Mode may be required when unrecoverable anomaly occurs

1- DPU shall be able to analyse HK parameter according to operating mode and limit check criteria.

2- The SPIRE instrument shall provide to the DPU all the useful HK required to perform health monitoring tasks.

This includes :

- detector bias
- calibration source current/temperature
- temperature (FPU, ...)
- FTS mechanism HK
  - current in winding (indicate open/short circuit)
  - translation OK Yes/No
- Chopper mechanism HK
  - current in winding (indicate open/short circuit)
  - moving part OK Yes/No
- command execution status report (sub-system or harness failure)
- scientific data consistency (?)
- .....

For engineering purposes other modes of operation have to be defined according to the IID-B list of scientific modes :

• the INIT mode is a mode the instrument enters after a boot process (following a power-on or a watchdog reset) or receiving a "Stop program" TC.
In this mode the S/W only execute a reduced number of TCs such as Load/Dump memory contents and Start program.
This mode is mandatory for S/W updates during on-ground or in-flight operations.

• the TRANSPARENT mode is a mode in which the instrument don't perform any data compression.
This mode is useful during ground operation such as integration activity and in-flight during Real-time commanding phases.
This mode may enabling the monitoring of glitches profile in order to update parameters of deglitching algorithm. In order to avoid TM saturation only a limited number of frames are acquired in this mode.
To be compliant with the TM peak rate (800 kbps) only part of the focal plane is acquired.

• a TEST mode is a mode in which the instrument generate known scientific data.
It enables to check the data path from DRCU to S/C.
This mode is useful during integration and verification activities and for in-flight diagnostic after a power-on or when a anomaly occurs in autonomy phase.

FUNCTION vs MODE of OPERATION CROSS TABLE (1)

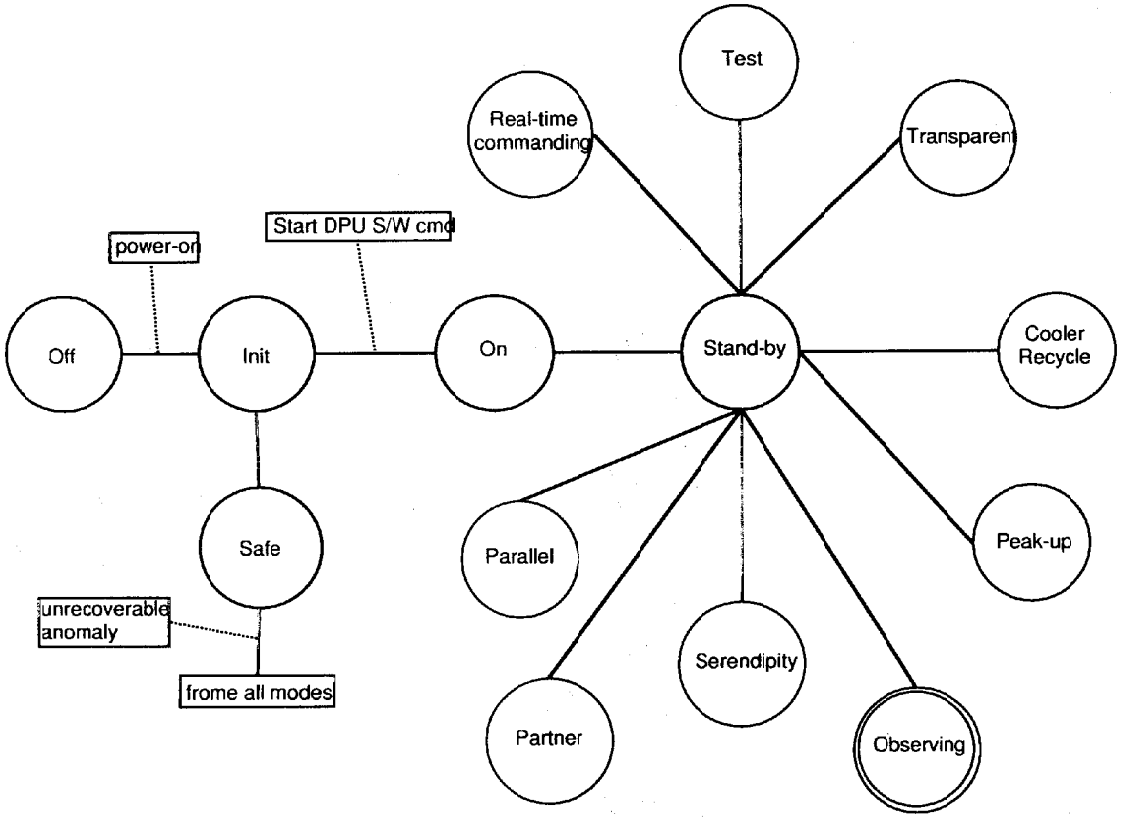
MODES / FUNCTIONS	Photo. chop	Photo. scan	Photo. partner	Photo. serendipity	Photo. parallel	Spectro full	Spectro narrow
0.3 Fridge Control							
FPU Tem. Regulation	Yes	Yes	Yes	Yes	Yes	Yes	Yes
H/K Acquisition	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Cal. Source Control	Yes periodic	Yes periodic	?	?	?	Yes	Yes
Photometer AS Processing	Yes	Yes	Yes	Yes	Yes	No	No
Photometer Seq/Mpx	Yes	Yes	Yes Low Res	Yes	Yes Low Res	No	No
Spectrometer Seq/Mpx	No	No	No	No	No	Yes	Yes
Spectrometer AS Processing	No	No	No	No	No	Yes	Yes
FTS Control	No	No	No	No	No	Yes High Res	Yes Low Res
Chopper Control	Yes Chop	Yes Scan	?	No	No	No	No
DRCU CMD/HK	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Data Time Stamping	?	?	?	?	?	?	?
SPU Data Reception	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Signal Demodulation	JPL option	JPL option	JPL option	JPL option	JPL option	JPL option	JPL option
Signal Deglitching	Yes	Yes	Yes	Yes	Yes	No	No
Frame Co-addition	Yes	Yes	Yes	Yes	Yes	No	No
Lossless Compression	No	No	No	No	No	Yes	Yes
SPU CMD/HK	Yes	Yes	Yes	Yes	Yes	Yes	Yes
SPIRE CMD Decod. + Exec.	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Data Proc. + Formatting	Yes	Yes	Yes Low Res	Yes	Yes Low Res	Yes	Yes
Telemetry Sending	Yes Full	Yes Full	Yes Part.	Yes TM/2	Yes Reduced	Yes Full	Yes Full

Photometer parallel mode is assumed to be the default standby mode (very to "standby mode")

FUNCTION vs MODE of OPERATION CROSS TABLE (2)

MODES / FUNCTIONS	Photo. peak-up	Jiggle photo.	Jiggle spectro	Standby	Real/Time CMD	Commisionnig Calibration	Cooler Recycle	On	Off	FPU op. at amb. temp.
0.3 Fridge Control	No	No	No	No	No	No	Yes	No	No	
FPU Tem. Regulation	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	
H/K Acquisition	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	
Cal. Source Control	?	Yes ?	Yes	?	?	?	No	No	No	
Photometer AS Processing	No	Yes	No	Yes	Yes	Yes	No	No	No	
Photometer Seq/Mpx	No	Yes	No	Yes Low Res	Yes	Yes	No	No	No	
Spectrometer Seq/Mpx	Yes	No	Yes	No	Yes	Yes	No	No	No	
Spectrometer AS Processing	Yes	No	Yes	No	Yes	Yes	No	No	No	
FTS Control	No	No	Yes Chop. Sync.	No	Yes	Yes	No	No	No	
Chopper Control	Yes Cross raster	Yes 2D steps	Yes 2D steps	No	Yes	Yes	No	No	No	
DRCU CMD/HK	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes s/w upload	No	
Data Time Stamping	?	?	?	?	?	?	No	No	No	
SPU Data Reception	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	
Signal Demodulation	JPL option	JPL option	JPL option	JPL option	JPL option	JPL option	No	No	No	
Signal Deglitching	Yes	Yes	No	Yes	Yes	Yes	No	No	No	
Frame Co-addition	Yes	Yes	No	Yes	Yes	Yes	No	No	No	
Loss-less Compression	No	No	Yes	No	No	No	No	No	No	
SPU CMD/HK	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes s/w upload	No	
SPIRE CMD Decod. + Exec.	Yes	Yes	Yes	Yes	Yes	Yes No limit check	Yes	Yes	No	
Data Proc. + Formatting	Yes Peak-up	Yes	Yes	Yes Low Res	Yes	Yes	Yes HK only	HK only	No	
Telemetry Sending	?	Yes Full	Yes Full	Yes High Reduction	Yes Full	Yes Full	Yes HK only	Yes HK only	No	

SPIRE Modes Transition Graph



Data Time Stamping :

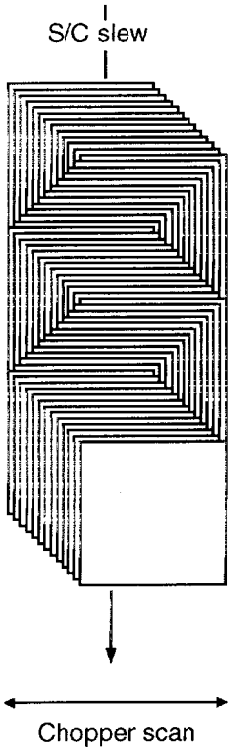
- **Implementation depends on required accuracy :**

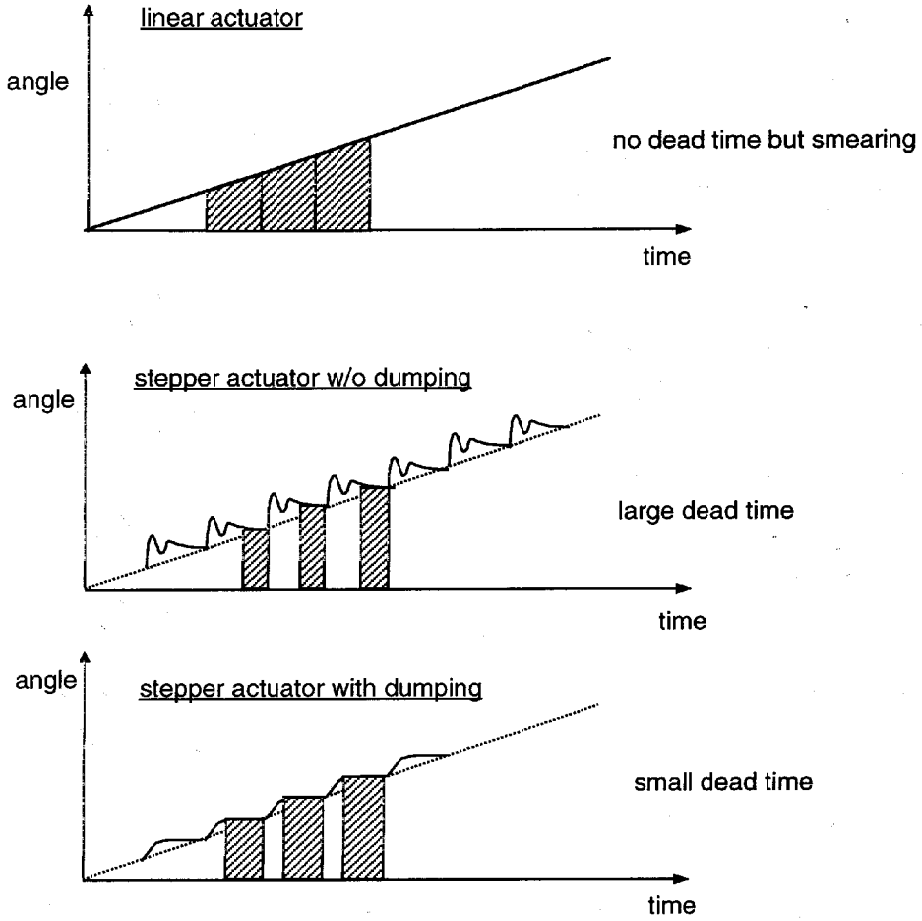
  1- if a high resolution is requested (µs or better) a hardware solution is preferred in the DRCU.

  2- if a low resolution is requested (ms or less) a software solution is to be considered in the SPU or DPU.

Requires a dedicated TBD interface with the OBDH ...

Chopper Operation in Photometer Scan Mode





• Sizes and Mass (IID-B 0.1)

Sub-system	Dimensions (mm)*	Mass (kg)
FSBAU	200 x 150 x 120	2.5
FSDRC	285 x 256 x 234	12
FSSPU	240 x 218 x 239	9
FSDPU	240 x 210 x 194	7

Note : Dimensions and mass do not include margins

• Power Dissipation (IIB-B 0.1)

Sub-system	Power Dissipation (W)
FSBAU	2,5
FSDRC	100
FSSPU	15
FSDPU	10

SPIRE DRCU Scientific Interface (1)

Need : High speed unidirectional serial line for DRCU scientific data transmission to the SPU or DPU

• <u>Data Format</u> based on 24 bits (MSB first) words including :

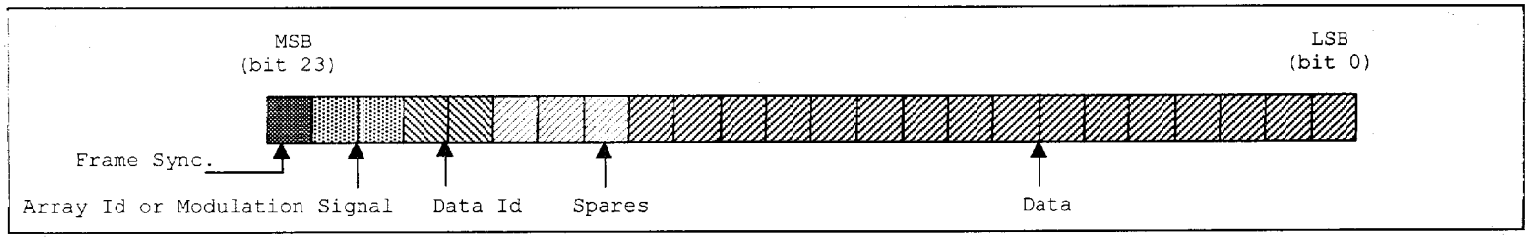
- **1 bit for frame synchronisation (Start of Frame or End of Frame)**

CEA/GSFC detector option only :

- **2 bits for array id (0 to 2 in photometer mode 0-1 in spectrometer mode)**

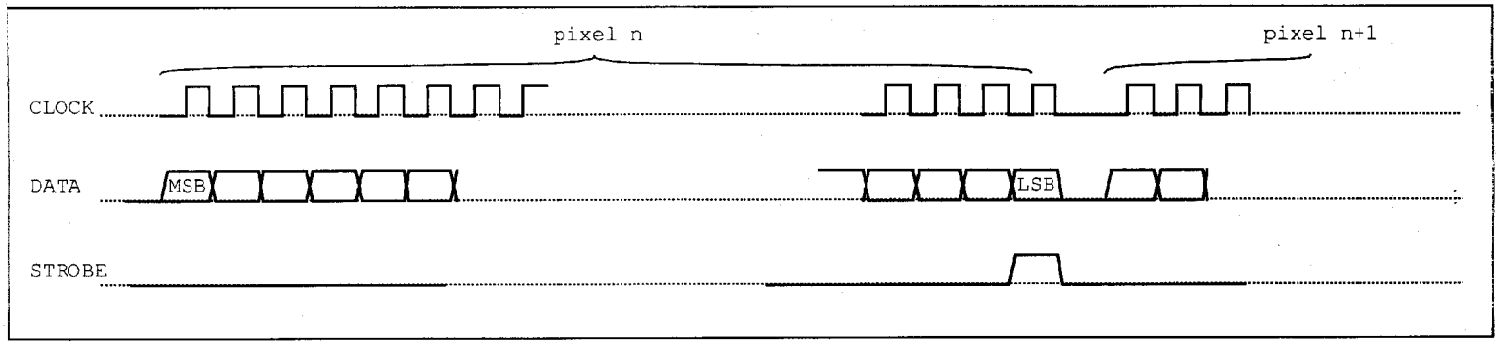
JPL detector option only :

- **1 bit for signal modulation synchronisation (demodulation in SPU or DPU)**
- **2 bits for data type id (pixel data or time stamping or chopper/FTS position)**
- **16 bits (TBC) for pixel data (up to 19 bits are available)**



SPIRE DRCU Scientific Interface (2)

• **Data Timing :**



• **Clock frequency :**

2 MHz for CEA & GSFC Array Options

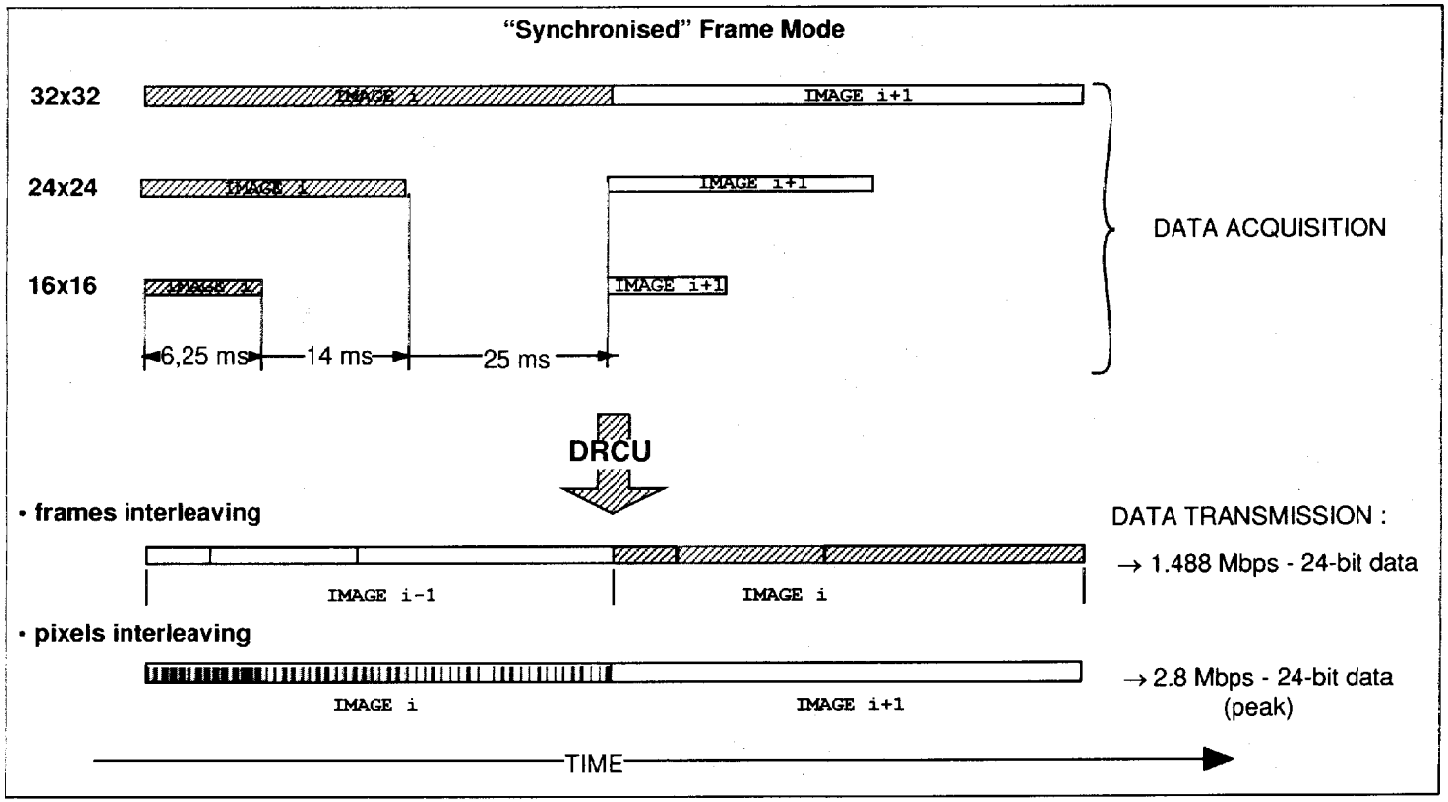
→ RS422 electrical standard is usable

20 MHz for JPL Array Option

→ electrical interface to be defined (RS422 is limited to 10 MHz)
- **use of LVDS (Low Voltage Differential Signalling) ?**
- **3 serial lines (instead of one) : one per bolometer type ?**
- **analog demodulation & filtering in the DRCU ?**

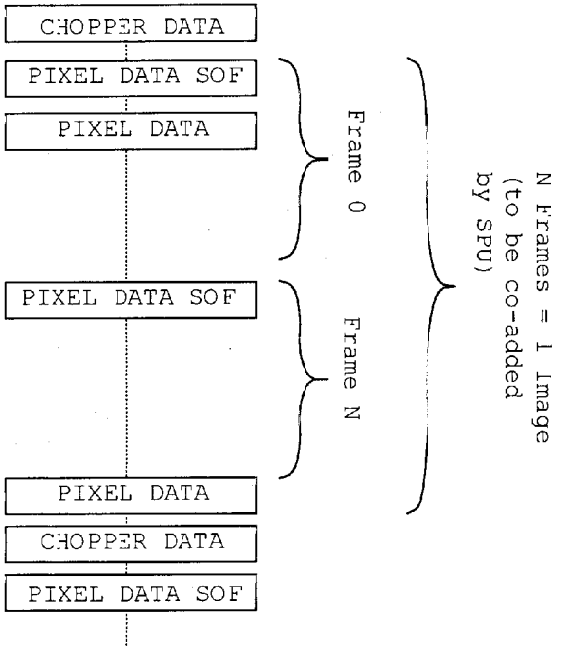
SPIRE DRCU Scientific Interface (3)

• **Frame Timing :**

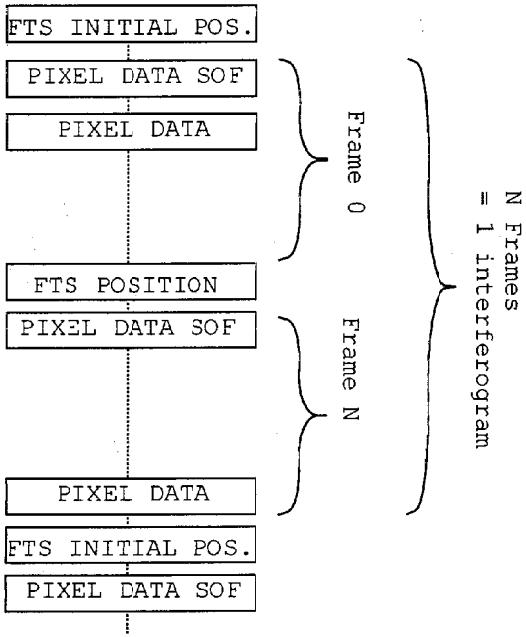


• **Data Flow** :

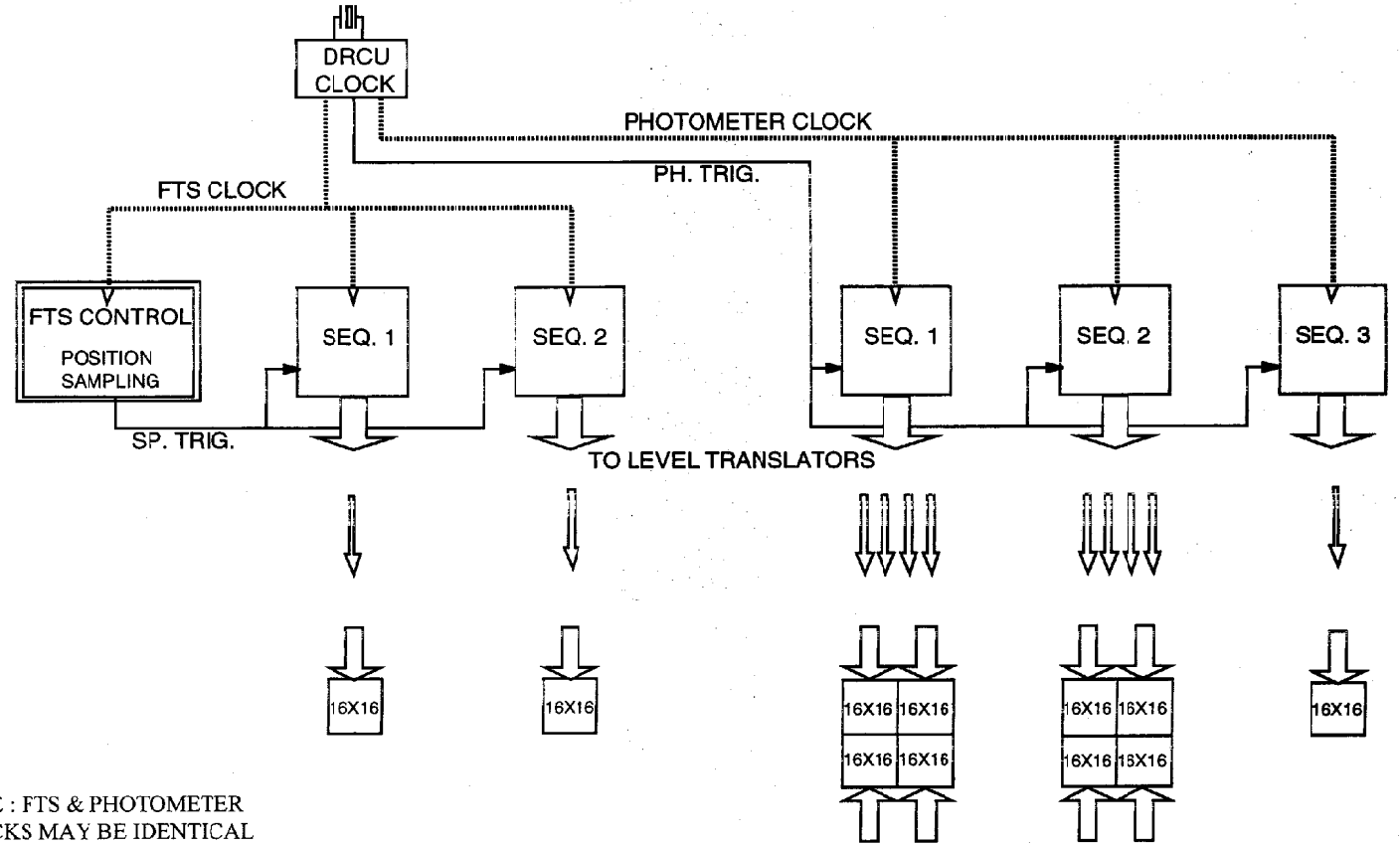
In Photometer Scan or Chop Mode



In FTS Mode

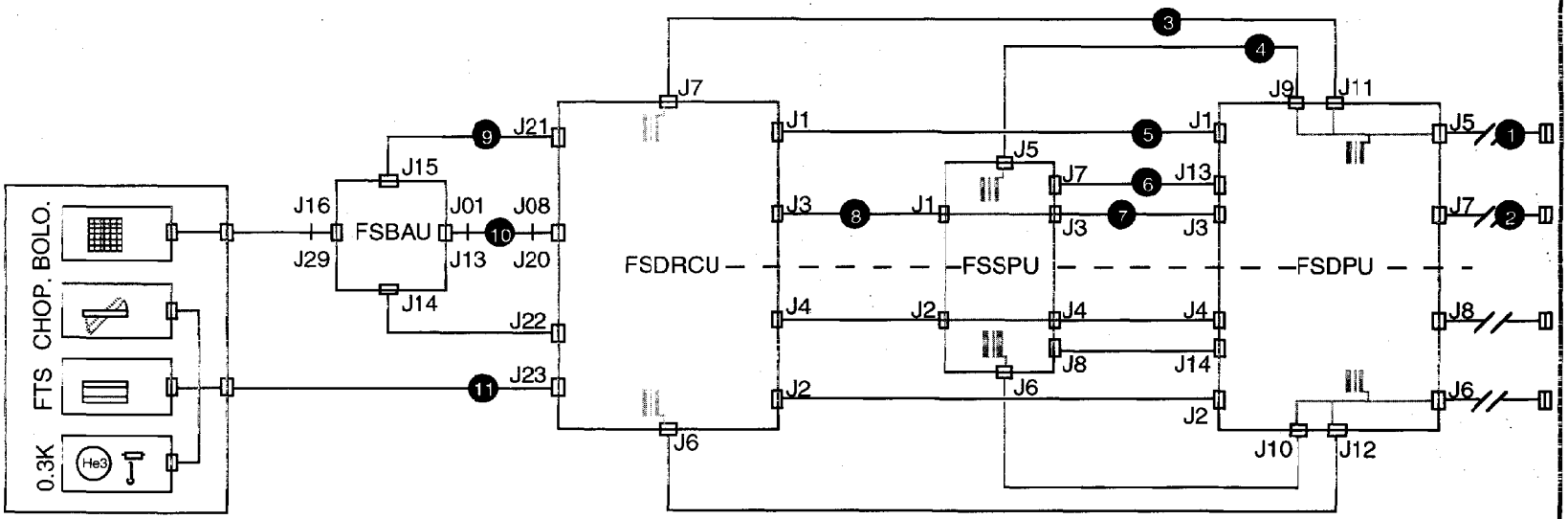


SPIRE DRCU Synchronisation Tree with FTS



NOTE : FTS & PHOTOMETER CLOCKS MAY BE IDENTICAL

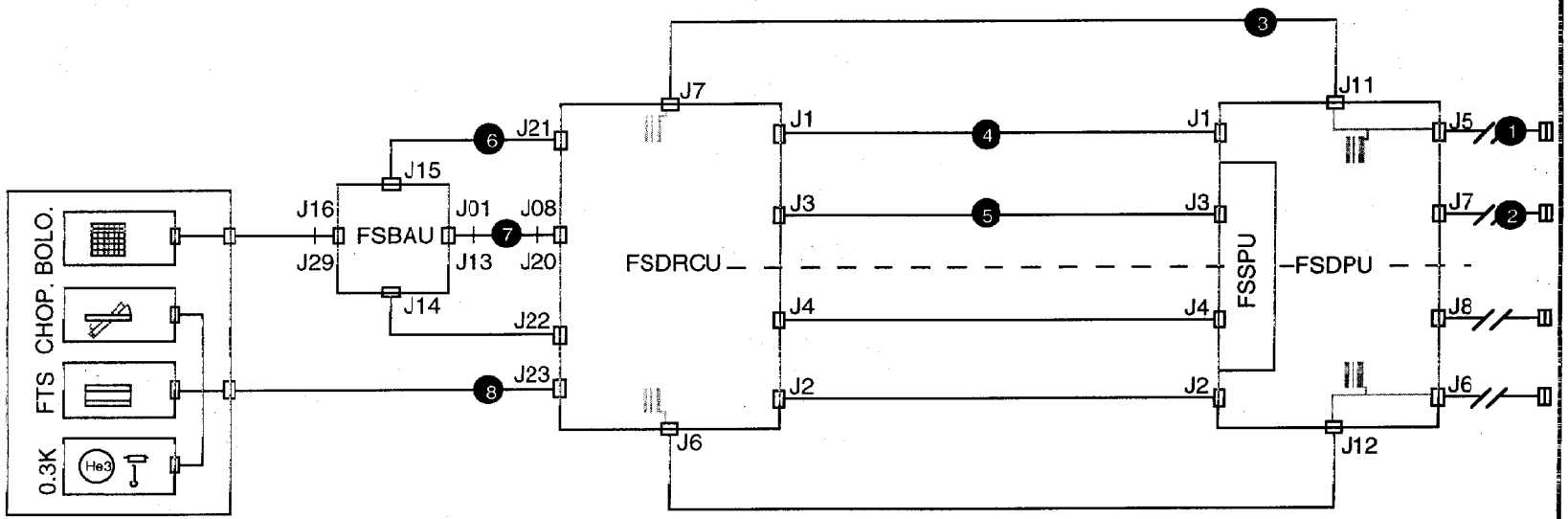
SPIRE ELECTRICAL CONFIGURATION
SPU H/W & S/W OPTION



HARNESS TYPES :

1. SPIRE CMD/HK
2. SPIRE PPWR
3. DRCU PPWR
4. SPU PPWR
5. DRCU CMD/HK
6. SPU CMD/HK
7. SPU DATA
8. DRCU DATA
9. BAU SPWR
10. BAU SIGNAL
11. MECHANISMS CONTROL + HK

SPIRE ELECTRICAL CONFIGURATION
SPU S/W ONLY OPTION

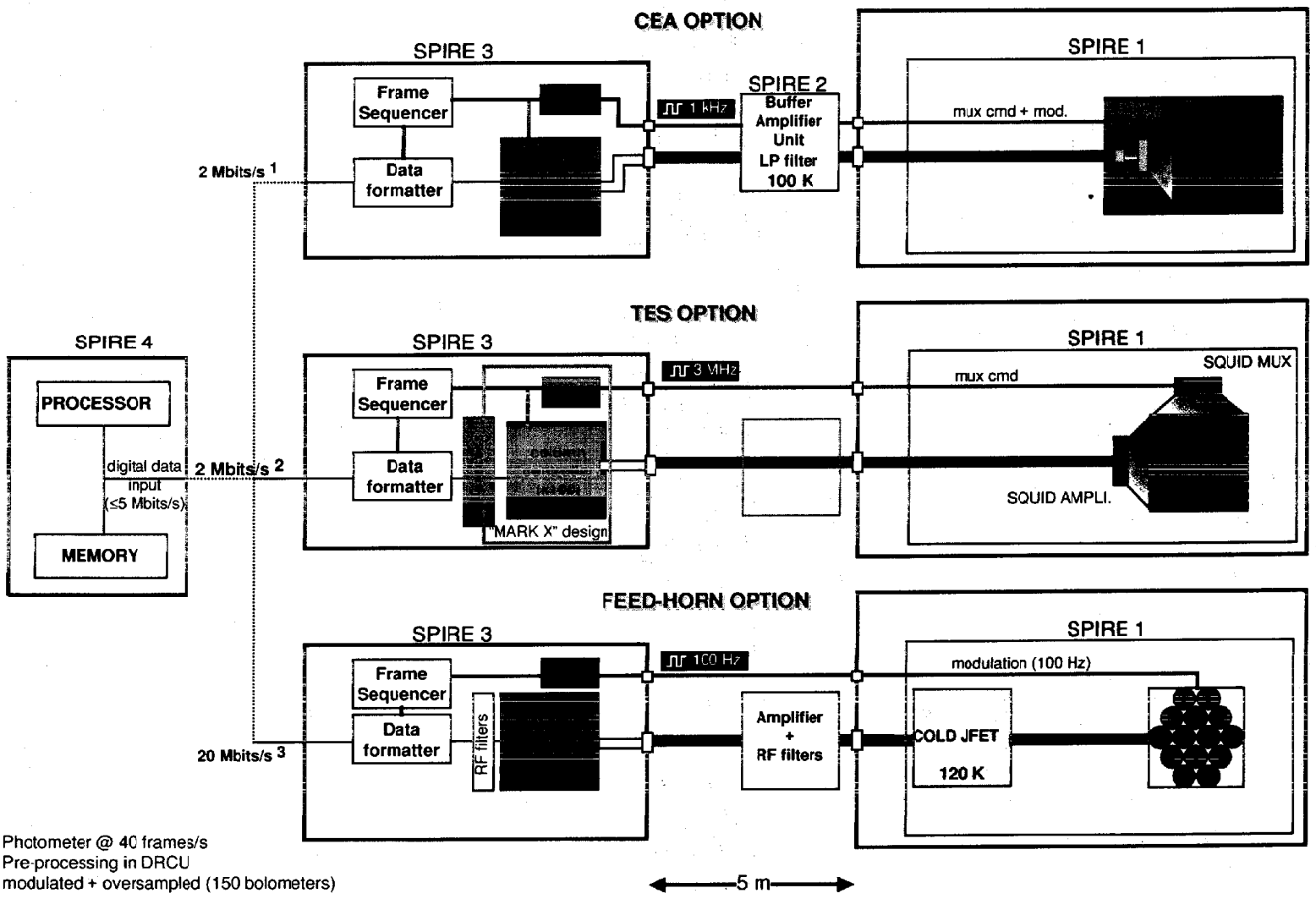


1. SPIRE CMD/HK
2. SPIRE PPWR
3. DRCU PPWR
4. DRCU CMD/HK
5. DRCU DATA
6. BAU SPWR
7. BAU SIGNAL
8. MECHANISM CONTROL + HK

FIRST / SPIRE

ELECTRONICS SYSTEM DESIGNS vs ARRAY OPTIONS

cea /SAp
24/03/99



1 : Photometer @ 40 frames/s
2 : Pre-processing in DRCU
3 : modulated + oversampled (150 bolometers)

SPIRE Signal Processing Input Data Rates vs Array Options

Assumption : microprocessor running at 20 MHz (clock period = 50 ns)

• CEA Option : 128000 24-bit words /s or one pixel every 8 µs

➔ 1 data acquisition every 160 microprocessor cycles
➔ DMA in not mandatory
➔ SPU have to perform data deglitching in photometer mode

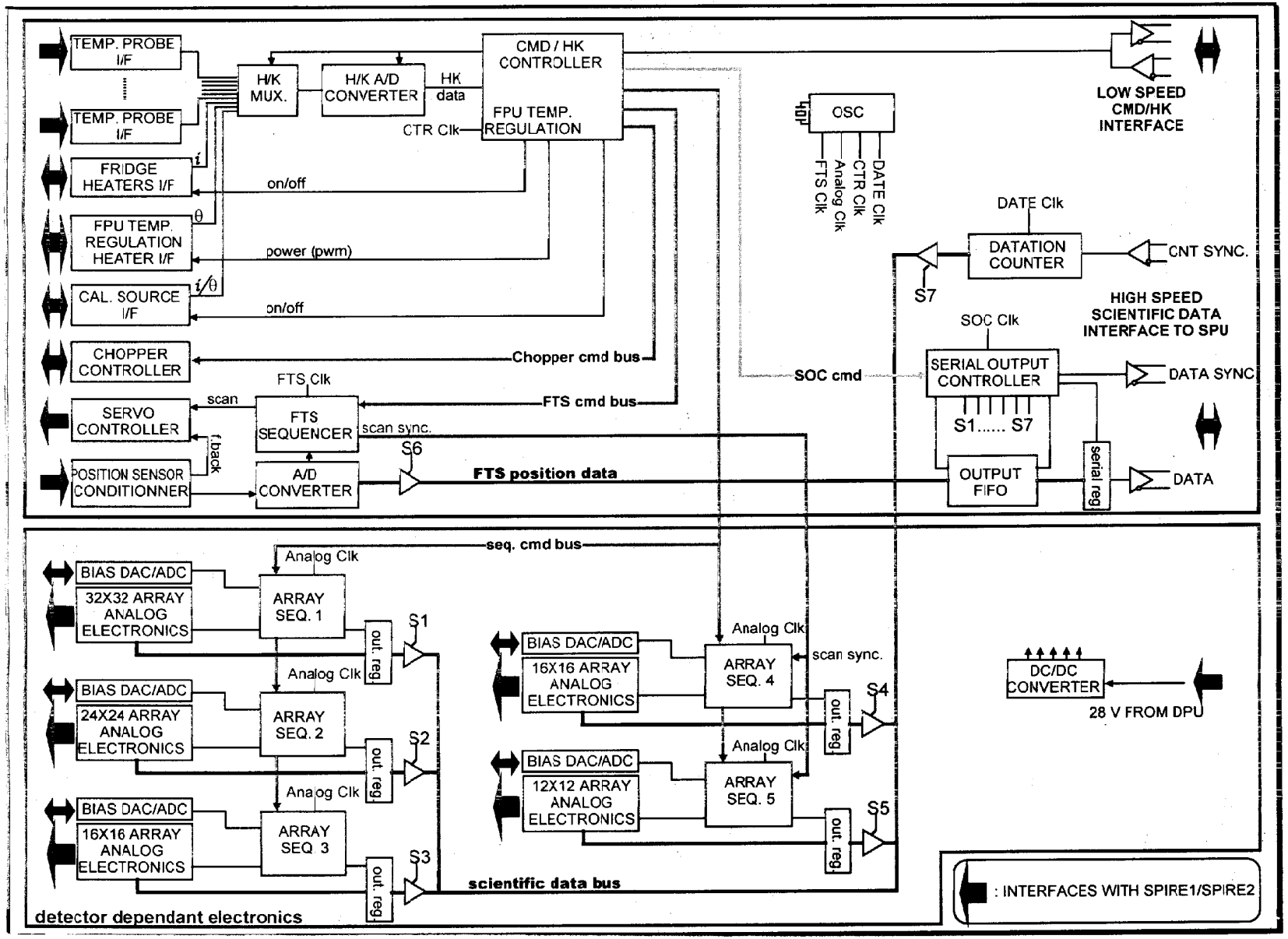
• JPL (Feed-Horn) Option : modulated and oversampled data gives 1.2 Mwords/s or one pixel every 830 ns

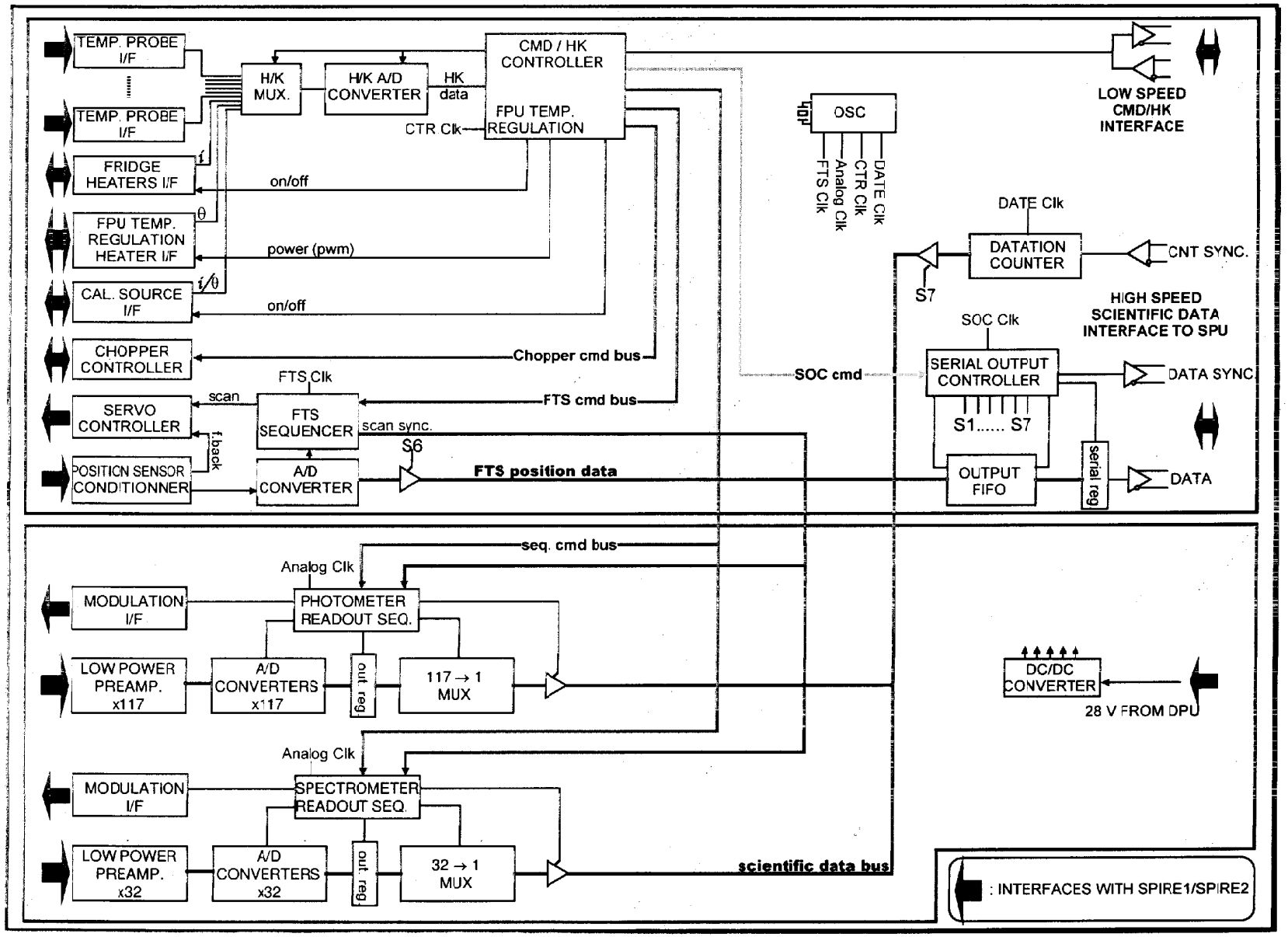
➔ 1 data acquisition every 16 microprocessor cycles
➔ requires DMA in the Signal Processing Unit
➔ SPU have to perform demodulation of incoming data
➔ SPU have to perform data deglitching in photometer mode

• GSFC (T.E.S.) Option : oversampled data gives 64 Mwords/s or one pixel every 15 ns

BUT : Pre-processing is now foresee in the DRCU to reduce DRCU output data rate and to deglitch pixel data

➔ same data rate as for CEA option
➔ no deglitching algorithm in SPU


TEMP. PROBE I/F
TEMP. PROBE I/F
FRIDGE HEATERS I/F
FPU TEMP. REGULATION HEATER I/F
CAL. SOURCE I/F
CHOPPER CONTROLLER
SERVO CONTROLLER
POSITION SENSOR CONDITIONNER
H/K MUX.
H/K A/D CONVERTER
HK data
CTR Clk
CMD / HK CONTROLLER
FPU TEMP. REGULATION
on/off
power (pwm)
on/off
Chopper cmd bus
FTS Clk
scan
FTS SEQUENCER
FTS cmd bus
scan sync.
f.back
A/D CONVERTER
S6
FTS position data
OSC
FTS Clk
Analog Clk
CTR Clk
DATE Clk
LOW SPEED CMD/HK INTERFACE
DATE Clk
DATATION COUNTER
CNT SYNC.
S7
HIGH SPEED SCIENTIFIC DATA INTERFACE TO SPU
SOC Clk
SOC cmd
SERIAL OUTPUT CONTROLLER
DATA SYNC
S1..... S7
OUTPUT FIFO
serial reg
DATA
seq. cmd bus
Analog Clk
BIAS DAC/ADC
32X32 ARRAY ANALOG ELECTRONICS
ARRAY SEQ. 1
out. reg
S1
Analog Clk
BIAS DAC/ADC
24X24 ARRAY ANALOG ELECTRONICS
ARRAY SEQ. 2
out. reg
S2
Analog Clk
BIAS DAC/ADC
16X16 ARRAY ANALOG ELECTRONICS
ARRAY SEQ. 3
out. reg
S3
detector dependant electronics
Analog Clk
BIAS DAC/ADC
16X16 ARRAY ANALOG ELECTRONICS
ARRAY SEQ. 4
scan sync.
out. reg
S4
Analog Clk
BIAS DAC/ADC
12X12 ARRAY ANALOG ELECTRONICS
ARRAY SEQ. 5
out. reg
S5
scientific data bus
DC/DC CONVERTER
28 V FROM DPU
: INTERFACES WITH SPIRE1/SPIRE2


TEMP. PROBE I/F
TEMP. PROBE I/F
FRIDGE HEATERS I/F
FPU TEMP. REGULATION HEATER I/F
CAL. SOURCE I/F
CHOPPER CONTROLLER
SERVO CONTROLLER
POSITION SENSOR CONDITIONNER
H/K MUX.
H/K A/D CONVERTER
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FTS cmd bus
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FTS SEQUENCER
scan sync.
S6
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A/D CONVERTER
FTS position data
OSC
FTS Clk
Analog Clk
CTR Clk
DATE Clk
LOW SPEED CMD/HK INTERFACE
DATE Clk
DATATION COUNTER
CNT SYNC.
S7
HIGH SPEED SCIENTIFIC DATA INTERFACE TO SPU
SOC Clk
SOC cmd
SERIAL OUTPUT CONTROLLER
DATA SYNC
S1..... S7
OUTPUT FIFO
serial reg
DATA
seq. cmd bus
Analog Clk
MODULATION I/F
PHOTOMETER READOUT SEQ.
LOW POWER PREAMP. x117
A/D CONVERTERS x117
out reg
117 → 1 MUX
DC/DC CONVERTER
28 V FROM DPU
Analog Clk
MODULATION I/F
SPECTROMETER READOUT SEQ.
LOW POWER PREAMP. x32
A/D CONVERTERS x32
out reg
32 → 1 MUX
scientific data bus
: INTERFACES WITH SPIRE1/SPIRE2

SPIRE Redundancy Concept (1)

Goal : to remove Single Point Failure in the instrument design and subsystem designs

May affects :
- **functions**
- **interface**

SPF definition depends on acceptable degraded mode of operation

Identification of SPF is the SPIRE instrument :	Criticity	Comment
• OBDH interface	Maximum	SPIRE is lost
• 28 V interface with S/C	"	"
• DPU DC/DC	"	"
• DPU Hardware (CPU, ...)	"	"
• 28 V interface with DPU	"	"
• SPU DC/DC	"	"
• DPU ⇔ SPU CMD/HK interface	"	"
• SPU → DPU scientific data interface	"	No scientific data ≈ some as above
• SPU Hardware (CPU, ...)	"	SPIRE is lost
• 28 V interface with DPU	"	SPIRE is lost
• DRCU DC/DC	"	"
• DPU ⇔ DRCU CMD/HK interface	"	"
• DRCU → SPU scientific data interface	"	No scientific data ≈ some as above
• DRCU CMD decoder/formatter	"	No scientific data / No FPU control
• DRCU scientific data formatter	"	No scientific data
• Spectrometer Sequencer/Multiplexer	High	No (or part of) spectrometer data
• Spectrometer Analogue Electronics	High	Part of spectrometer data

SPIRE Redundancy Concept (2)

• Photometer Sequencer/Multiplexer	High	No (or part of) photometer data
• Photometer Analogue Electronics	High	Partial field of view/spectral range loss
• FTS control	High	No interferogram
• Chopper Control	?	Only S/C scanning remains
• Calibration Source Control	?	Reduction of scientific performance
• Fridge Control	High	No fridge recycling / FPU temp. rises
• FPU temperature regulation	?	Reduction of scientific performance
• BAU power supply (from DRCU)	Maximum	No scientific data
• BAU → DRCU analogue interface	High	Partial field of view/spectral range loss
• BAU hardware	High	Partial field of view/spectral range loss
• FPU → BAU analogue interface	High	Partial field of view/spectral range loss
• DRCU ⇔ Detector Array interface	?	Partial field of view/spectral range loss
• DRCU → Chopper (Scan signal)	High	Only S/C scanning remains
• Chopper → DRCU (Position signal)	Medium	
• DRCU → FTS (Scan signal)	High	No interferogram
• FTS → DRCU (Position Signal)	Medium	Reduction of scientific performance
• FPU temperature probe → DRCU	?	Reduction of scientific performance
• DRCU → Fridge heater	High	No fridge recycling / FPU temp. rises
• Fridge temperature probe → DRCU	?	No feed back when recycling fridge

SPIRE Redundancy Concept (3)

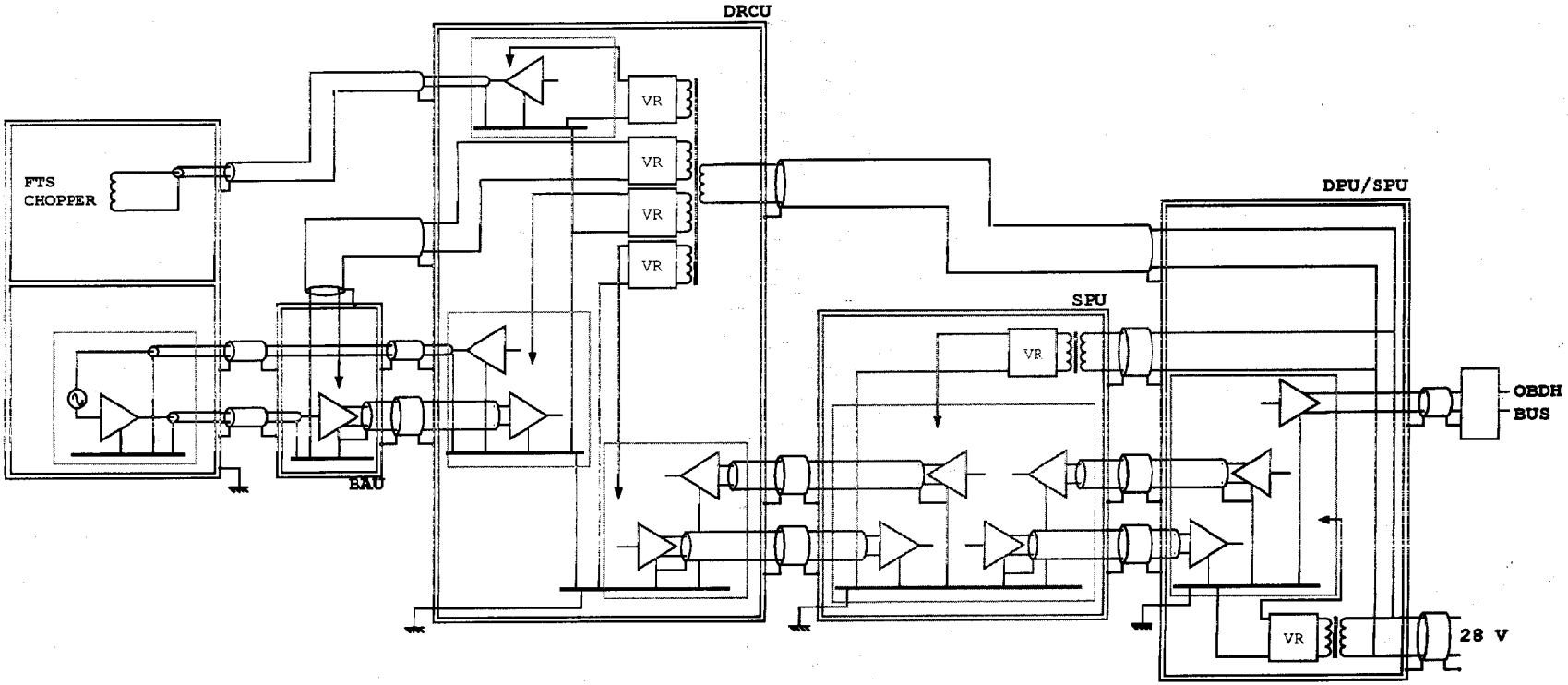
• **Conclusion** :

➔ **DPU / SPU are fully redunded**

➔ **DRCU is partially redunded :**

• CMD/HK, + FTS Control, + Scientific Data Formatter/Interface, + Fridge Recycling, + DC/DC, + Secondary supply for BAU	**are redunded**
• Chopper Control, + FPU temperature Regulation, + Calibration source Control	**may be redunded**
• Analogue Electronics + Sequencers/Multiplexer	**are not redunded**

SPIRE GROUNDING DIAGRAM



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