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BOL | CEA | N | 0029.10

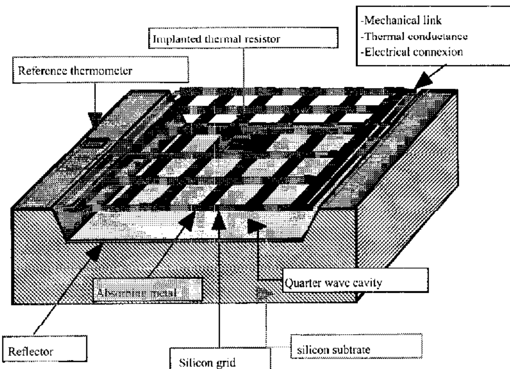
# CEA planar bolometer array
# Technical description.

L. Rodriguez,
P. Agnese,

C. Cara,
L. Vigroux

## 1 Technical description:

Monolithic bolometer arrays equipped with their readout circuit.
The pixel is made up of a monocristalline silicon grid (5 µm thick or less) suspended by micronic beams to ensure thermal insulation. The grid is suspended above a quarter wave cavity with a metallic reflector base. This vertical assembly allows a resonant absorption of the electromagnetic waves in a metallic layer deposited on the self-suspended silicon grid. The vertical resonance profile absorption is broadened by horizontal resonance induced by a defined half wave metallic pattern. The grid centre is reserved for the thermometric sensor processing. On one side of the pixels, a second thermometer is implanted in the thick substrate. The electrical signal is given by the unbalance between the two thermal resistance bridge.

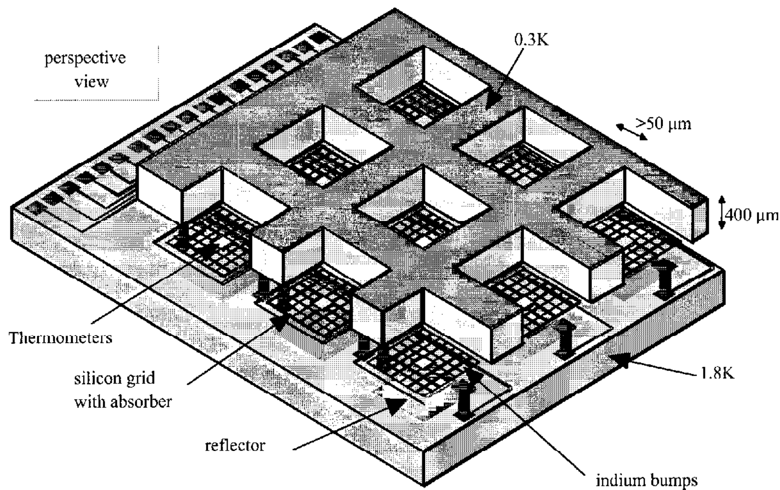



Resonnant absorption detector principle.

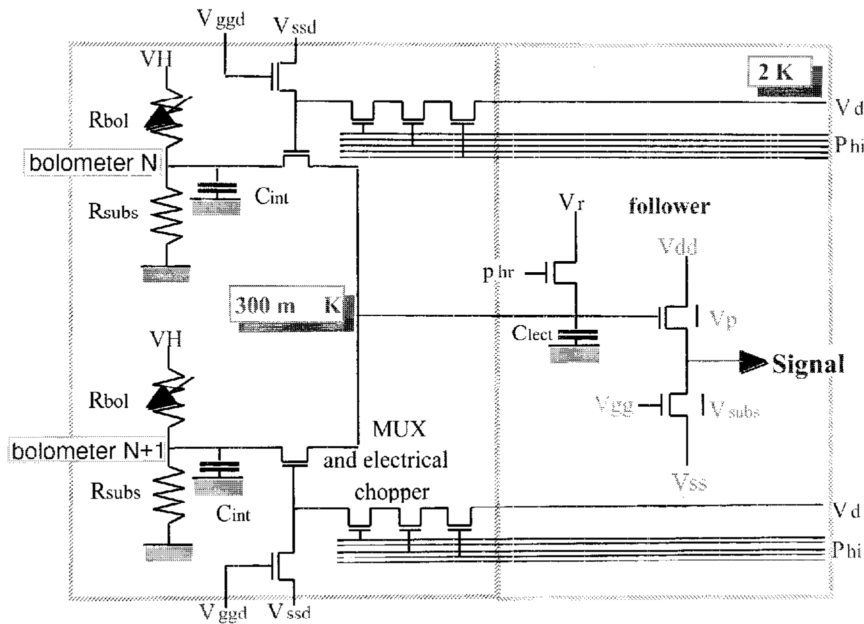
Thermal sensors are obtained by Phosphorus implantation with 50% Boron compensation. At 300 mK, the electrical conduction behaviour is consistent with hopping conduction . For homogeneity criteria in response through arrays (flat spatial response) easy multiplexing and power dissipation at cold stage a very high impedance for sensors was chosen (10-100 GΩ).

Two metal absorbers are currently tested WN an TiN with respective thickness of 500 and 380 Å. Both types are found superconductive at 300 mK for DC current but still keep the absorptive properties above 200 GHz.

Many pixels of this type can be assembled by collective manufacture to obtain a 2-D array of high complexity (depending mainly of the relative size of the pixel to the silicon wafer). For BOL, the arrays will be 32 x 32, 24 x 24 and 16 x 16 pixels.




According to simulations on a 3-D Maxwell code, the absorption profiles can be tailored to obtain a large coefficient ( over 90 % ) in a 200-250 µm range around the central peak.
Silicon grids are obtained by etching of a 400 µm silicon wafer. After implantation and metallisation, the silicon grid is hybridised to an interconnection circuit by indium bumps. The bumps are used to extract the signal from bolometers and to adjust the cavity length. On the interconnection circuit individual gold patches under each grid are the reflectors for the resonant absorption. The signal is leaded to the cold read out circuit (2 K) by metallic strips on the interconnection circuit. In between a multiplexer operating at 300 mK (8->1) limits the read out circuit to **128** electrical followers.
The read out circuit is an integrated C-MOS follower close to the bolometer array. The thermal decoupling is ensured by Kapitza thermal resistance at indium bumps boundaries.
The multiplex function is obtained by C-MOS circuits in gate mode at 300 mK welded on the interconnection circuit. We present below the example of two pixels connected to the same follower in the reference voltage chopping mode.




The measured thermal sensitivity (1.5 µK/ÃHz) of the thermometers imposes a large thermal impedance between the bolometer and the silicon substrate to achieve the desired NEP. The thermal bandpass is then limited to 15 -20 Hz.
The electric bandpass of the thermometer is also limited to 20 Hz by the impedance of the thermistors and a designed capacity to reduce the detector noise band. High impedance thermistors allows high bias levels and then give high output signal at the follower (no necessity to large gain electronics simplifying the electrical design).

**1.1-On (Observe):**
The detectors will be operated in photometric or spectroscopic mode. The multiplex will be operated at around 200 Hz/pixel giving a frame frequency around 15 Hz. The bias current will be chosen in such a way that the joule dissipation will be close to the photon heat load on the bolometer (1 pW).
In photometric mode three operational modes can be foreseen: telescope optical chopping, bias square modulation or MUX internal modulation. The two first modes are well known and I will not describe them, the later mode is permitted by the multiplex scheme discussed above. At the MUX level all signals can be compared to an internal voltage reference level at high frequency (>>200 Hz) .

**1.2-Off :**
Housekeeping only, He cooler off, detectors bias off, Focal plane at 2 K.

**1.3-Fridge Recycling :**
Detectors off, cold read out off, He cooler heater on, HSK and Warm electronics on.

**1.4-Standby :**

In the standby mode the bias must be maintained ( 1 pW at the 300 mK level) and the sorption fridge at 300 mK. The cooler is then in function at the recycling cost on the 2 K bath.

**1.5-Parallel :**
No partial use of the arrays is available. The data compression or reduction must be done at the real time processor level (TBC).

## 2. -Specifications:

### 2.1.1-Operating temperature:
The detector arrays are designed to work at 300 mK.

Cold read out circuit will operate at 2K as close as possible to the focal plane unit to minimise the electrical capacity of the high impedance circuit.

### 2.1.2-Power consumption for each mode:
**Detector (300 mK):**
The power consumption at the detector level is Joule effect on the thermistors. The joule dissipation amount is close to the background heat load from the telescope (1 pW). C-MOS multiplexers at 300 mK in gate mode are expected to be well below the conduction heat load from the 2 K stage (TBC).

**Cold read out electronics (2K).**
**-On**
Each C-MOS follower dissipates 5 μW on the 2 K stage. For 128 followers the total dissipation will be around 0.7 mW.

**-Standby**
TBD

**-Off**
0 mW

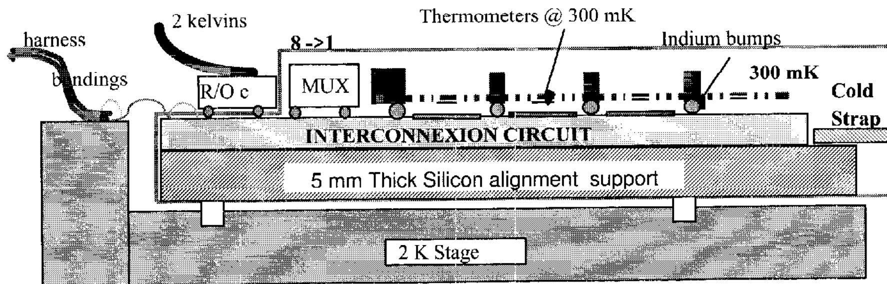
### 2.1.3-Harness requirements:

Three harnesses are needed to connect the detector arrays to the warm electronics. Two will be devoted to the signal lines, redundant biases, reference voltage lines and focal plane temperatures probes. The last harness for the digital signals: clocks, address code to the MUX and on/off voltages for the read out electronics. No peculiar type of wiring needed inside the BOL box: at the follower output the signals are low impedance, temperature is almost uniform in the instrument. Link to the 4 K stage and warm electronics box TBC.

### 2.1.4-Electromagnetic compatibility:

DC-Mean earth value or lower.
AC- Less than $10^{-5}$ teslas in the range 5-1000 Hz.
RF- TBD

**2.2-Thermal model:**
The thermal load on the 300 mK stage due to conduction from 2 K stage will be around 5 μW per array.




The read out circuit must be at 2 K, but close to the IC to control and minimise the electrical capacity and then the signal bandpass.

It will be the attached to the IC by indium bumps. The indium bumps ensure the electrical coupling and the thermal interface. Each bump is soldered on a $(15\ \mu m)^2$ gold pad ( can be made to 10 μm) on the IC circuit.
The thermal resistance according to Paul Richards's paper for a metal insulator interface (here indium or gold / silicon) is :

$Rb=B/T^3$ , with B typical. value 20 $K^4 cm^2/W$.

The most resistive interface is at 0.3K , we have then, per bump,

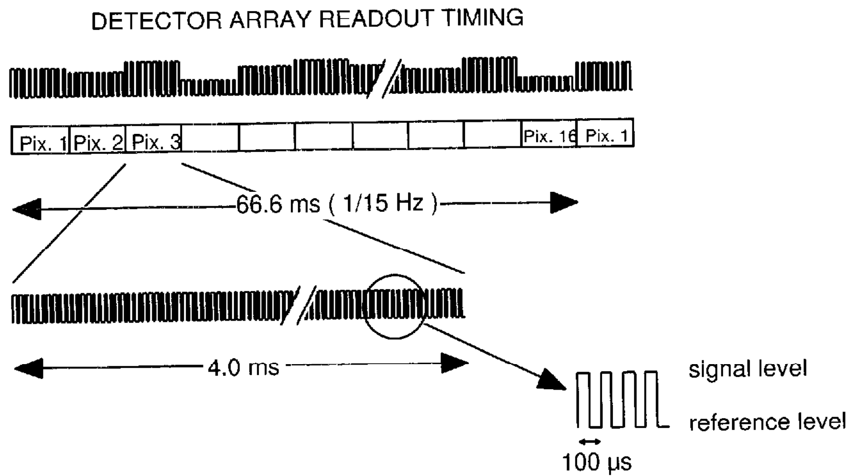
$G=(2.25e\text{-}6\ cm^2 * 0.3^3/B)\ (W/K) * 2K= 6.\ e\text{-}9\ W$

For 200 bumps, we obtain 1.2 μW per array. In this calculation, we did not take in account the micron metal strips to the MUX which length depend of the pixel position. assuming a factor 4, we expect to be under 5 μW for a 1024 pixel array ( worst case).
The thermal decoupling of the harnesses will be obtained by resistive metal strips on a loose polyimid membrane between interconnection circuit and harness fixation plate. Electrical coupling to the strips by gold bondings.

**2.3-Data Rate and Processor requirements:**
Frame time = 15 Hz. The data rate will be between 7680 and 27840 pixels /sec :

| | array size | Frame freq | Pixel rate |
|---|---|---|---|
| | | Hz | Hz |
| imager | 32 x 32 | 15 | 15360 |
| | 24 x 24 | 15 | 8640 |
| | 16 x 16 | 15 | 3840 |
| | | | |
| total | | | 27840 |
| | | | |
| Spectrometer | 16 x 16 | 15 | 3840 |
| | 17 x 16 | 15 | 3840 |
| | | | |
| total | | | 7680 |

**2.3.1-Anticipated read out frequency / mode:**
15 Hz / frame x 8 channels = 120 Hz modulated at 10 kHz for 1/f follower & cold electronics noise removal.
Hereafter a scheme of the read out sequence.




**2.3.2-Number of bits required for digitising the outputs:**
14 bits (TBC).

**2.3.3-On board processing and memory requirements**
**If telemetry = 40 kbits/s**
**Photometric mode:**
**Memory :** 2 bytes images for 3 arrays (1856 pixels)= 7,5 Kbytes @15 Hz.
**Compression processing:** Raw data = 3.7 Kbytes every 60 ms = 445 440 bits/sec.
Needed compression: x 12 minimum, probably more (degliching table).

**spectroscopic mode:**
**Memory:** 16 bits images x 4200 samples in the 2 arrays (512 pixels), 8 Mbytes for co adding

**Compression processing:** Raw data = 1024 bytes/60 ms. Needed compression Å 4 ( co-addition). Deglitching at ground level (TBC).

### 2.3.4-Final telemetry rate:

40 kBits / second.

### 2.3.5-Commanding:

Cold read out circuit and bias on/off, reference Voltage.
MUX addressing circuit
For a 8 - > 1, three wires within 5 ,
for a 16 -> 1, 3 wires within 6.
Clock signal for MUX internal modulation (10 kHz).

### 2.4-Mechanical support:

TBD

### 2.4.1-Outline of the anticipated mechanical interface to the cold stage:

TBD

### 2.4.2-Mass of the cold array and electronics:

Depending of the mechanical support ( isocam LW detector array Å100 g)

### 2.4.3-Handling specifications:

Qualification or Flight Detectors must be handled in a class 1000 (or better) clean room.

### 2.4.4-Outline thermal interface:

Flexible heat strap to the $^3$He fridge. The cold strap will be bolted to the thick silicon support.

### 2.5-Expected performances:

For 0.5 $\lambda$/**D** pixels $R_{bol}=10^{12}$ ½. Optimal bias 0.22 V.
a) under a photon flux of Q = 0.5 pW ($\lambda$ = 500 $\mu$m) :

$NEP_{det}$ =4 $10^{-17}$ W/ÃHz or $NEP_{det}$ = 1.4 $NEP_{blip}$

b) under a photon flux of Q = 0. pW :

$NEP_{det}$ =1.8 $10^{-17}$ W/ÃHz .

### 2.6-Development schedule:

### 2.6.1-Heritage:

Bolometer planar arrays: industrial manufacture of 64 x 256 resonant detector arrays in the 6-10 $\mu$m spectral range at room temperature.

2 K Detectors: manufacture of ISOCAM LW detector arrays.

2 K Electronics: ISOCAM C-MOS cold read out followers.

Warm Electronics: CASSINI / CIRS warm read out and analog signal processing for a 10 pixel HgCdTe PV detector array. The CIRS warm electronics was fitted to a Fourier Transform Spectrometer centred around the 50 Hz in a 10 Hz audio range.

**2.6.2-Outline development plan :**

December 97-January 98: Electrical and optical performances tests of 5 x 10 arrays .

January-June 98: manufacture of a representative multi- layer interconnection circuit with the cold MUX and read out followers.

February-October 98: manufacture of 10 x 10 uniform pattern filled detector arrays ( including mesh, crosses and capacitive loops patterns) optimised at 350 µm. Manufacture of mesa diffused thermometers arrays. Comparison with multi-implanted technique.

October 98-February 99: test of arrays performances.

June 98-February 99: Prototype Warm electronics coupling.

February-October 99: manufacture of 32 x 32 arrays optimised to 350 µm absorption.

October-December 99: Extensive tests of arrays performances.

**January 2000: selection of BOL detector arrays.**

February 2000-December 2000: manufacture of other arrays (other wavelength & FTS arrays) Scientific models. Manufacture of other cold read out circuits (QM & FM).
QM level space qualification. QM Integrated warm electronics manufacture

January-December 01: integration and test in the Qualification model of the instrument.

September 01-September 02: Manufacture of flight arrays.

September 01-December 02: FM integrated warm electronics manufacture.

February 02-December 02: Detectors Tests & Qualification.

January-December 2003: Integration and test in the Flight Model .

June 2003-June 2004: Integration and tests for the flight spare.

**2.6.3-Flight/flight spare devt. Program:**

See 2.6.2.

**2.6.4-Ground test and calibration:**

TBD

### 2.6.5-Risk assessment:

| **0.5 λ/D Filled detector arrays** | | | |
|---|---|---|---|
| **Item** | **Development status** | **Risk to system** | **Devt risk** |
| self standing grids manufacture | proven | none | none |
| implanted thermometer on thin substrate. | Performances achieved on thick silicon | higher heat capacity<br>therm bandpass < 20 Hz | medium |
| Mesa thermometers | Chip design phase | improve performances and yield of implanted thermometers<br>therm bandpass > 20 Hz | medium |
| Thermal impedance to heat sink | prototypes to be tested | therm bandpass < 20 Hz | low |
| Metal Absorber & pattern def | optimisation phase passivation evaluation. | lower quantum efficiency, narrower spectral band | medium |
| Cold MUX @ 300 mK | in operation on ISO detect. at 2 K | Noise performances TBC | low |
| C-MOS Follower @ 2K | in operation on ISO detect. | none | none |

### 2.7-Product assurance:

The SAp detector arrays and electronics will be delivered with a product assurance document. Our assurance quality plan is compatible with ESA, NASA and CNES plans.

### 2.7.1-Space qualification:

The detectors will be space qualified.

### 2.7.2-Yields Processing :

No information yet.

### 2.7.3-Materials:

Detector substrate: p monocristalline silicon. Isolation $SiO_2$.

Absorber metal: TiN or WN
Thermometer: Phosphorus (doping 3 $10^{18}/cm^3$ ) 50% Boron compensation.
Metal vias: Al ,TiN or WN.
Hybridization: indium
Pads & reflectors: Gold, Ni, Ti, Pd, Al, $Si_3N_4$.
Electrical Connection to the 2 K stage: manganin/Au on Kevlar.
Support structure Ti or Mo (TBC).
Thermal decoupling from the support structure (TBD)

### 2.7.4-Aging:

No information yet.

### 2.7.5-Environmental and handling requirements:

No information yet.

## 2.8-Special spacecraft requirements:

No information yet.