FIRST/ESA/M/033-10

MPE	**Minutes of Meeting**	Doc. Nr. : Page : 1 of
Subject: FIRST COMMONALITY MEETING		Date : 13-11-97 Place : ESA HEADQUARTERS PARIS

Participants:			Distribution:
Name	Organisation	Signature	all present
1. Ken King	RAL.		cc:
2. Albrecht Poglitsch	MPE		
3. JOSE M. HERREROS	IAC		es
4. Peter Roelfsema	SRON		
5. Douwe Beintema	SRON		
6. Benoy Thomas	LAL/ORSAY		
7. Renato Orfei	IFSI-CNR		
8. RICCARDO CEROLLI	" "		
9. CARLO ROSOLEN	OBSERVATOIRE PARIS		
10. OTTO H. BAUER	MPE		
11. Roger PONS	CESR		
12. Jacques Narbonne	CESR		
13. Emmanuel CAUX	CESR		
14. Hans Schaye	ESTEC		
15. Jacques CHARRA	IAS		
16.			
17.			
18.			
19.			
20.			

	Action item, responsible, due date

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The following points should be addressed:

(1) Digital electronics
Each team could give a short presentation concerning the overall concept, interfaces and modes of operation.

(2) Spacecraft interface simulator

(3) On-board microprocessor(s)

(4) On-board programming language

(5) Software development environment and standards

(6) Software validation facilities

(7) Instrument on-board software including instrument autonomy

(8) Memory load and verification

(9) Instrument commanding: Instrument Command Sequences (ICS's), Macros

(10) Instrument software simulator

(11) Instr. EGSE: Real-Time Assessment (RTA), Quick-Look Analysis (QLA)

(12) Test sequence language

(13) Commonality between Instrument Level Tests (ILT), System Tests and Operations

(14) FIRST Integrated Network and Data Archive System (FINDAS)

Subject: [Fwd:Questionnaire on the needs of industry for pre-buying 31750]]
Date: Mon, 10 Nov 1997 09:02:16 -0800
From: "F. Peran" <fperan@crisa.es>
Organization: CRISA
To: Jose Miguel Herreros <jhl@ll.iac.es>, Fleming Pedersen <pedersen@crisa.es>, "Javier G. Huete" <jhuete@crisa.es>

Estimado Jose Miguel:

Adjunto te envio la encuesta realizada en septiembre de este aqo con objeto de anticipar la compra de microprocesadores MA 31750 (y circuitos auxiliares) de GEC PLESSEY antes de que cese su produccion.

Lo mas interesante del asunto es que excluyen programas como FIRST y PLANCK, por haberse realizado ya provision por las respectivas CPPA.

Podrias recabar informacion en la ESA de si esta provision incluye a los instrumentos?.

MA31750 es la mejor opcion como procesador para REBA.

Saludos.

Francisco Peran.
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Francisco Peran
CRISA
Tlf: 34-1-8068753

Subject: [Fwd: Questionnaire on the needs of industry for pre-buying 31750]
Date: Thu, 06 Nov 1997 15:31:56 +0100
From: Jose Moreno <moreno@crisa.es>
Organization: CRISA
To: fperan@crisa.es

2-3 years.

(N.B. Several options are under consideration to replace GPS parts. However such options cannot give results before a few years. As a consequence, recourse to pre-buy has been viewed by all participants in the meeting as a unavoidable policy for the next years).

In order to act quickly (the GPS situation making it necessary to act as soon as possible), it was decided to circulate a questionnaire to evaluate the needs of industry under the conditions defined below. The purpose is to obtain good prices from GPS by grouping the purchases of ESA and the companies (which, of course does not mean that ESA or the companies cannot purchase from GPS individually).

We ask you to fax your answer to this questionnaire to Eurospace (attention Mr Marcel Toussaint) as soon as possible. By September 25th, the replies will be communicated to Mr Creasey (ESTEC). They will be treated in confidentiality (meaning that only the global figures but not the figures from the individual companies will be communicated outside Mr Creasey's division). Furthermore, the figures given will imply no committment, being preliminary evaluations.

As soon as Mr Creasey's team will have received and analysed the replies, they will contact GPS to organise with them a meeting where prices and time of orders and deliveries will be discussed in a preliminary manner, but on the base of the evaluated needs. Eurospace members will be represented at that meeting.

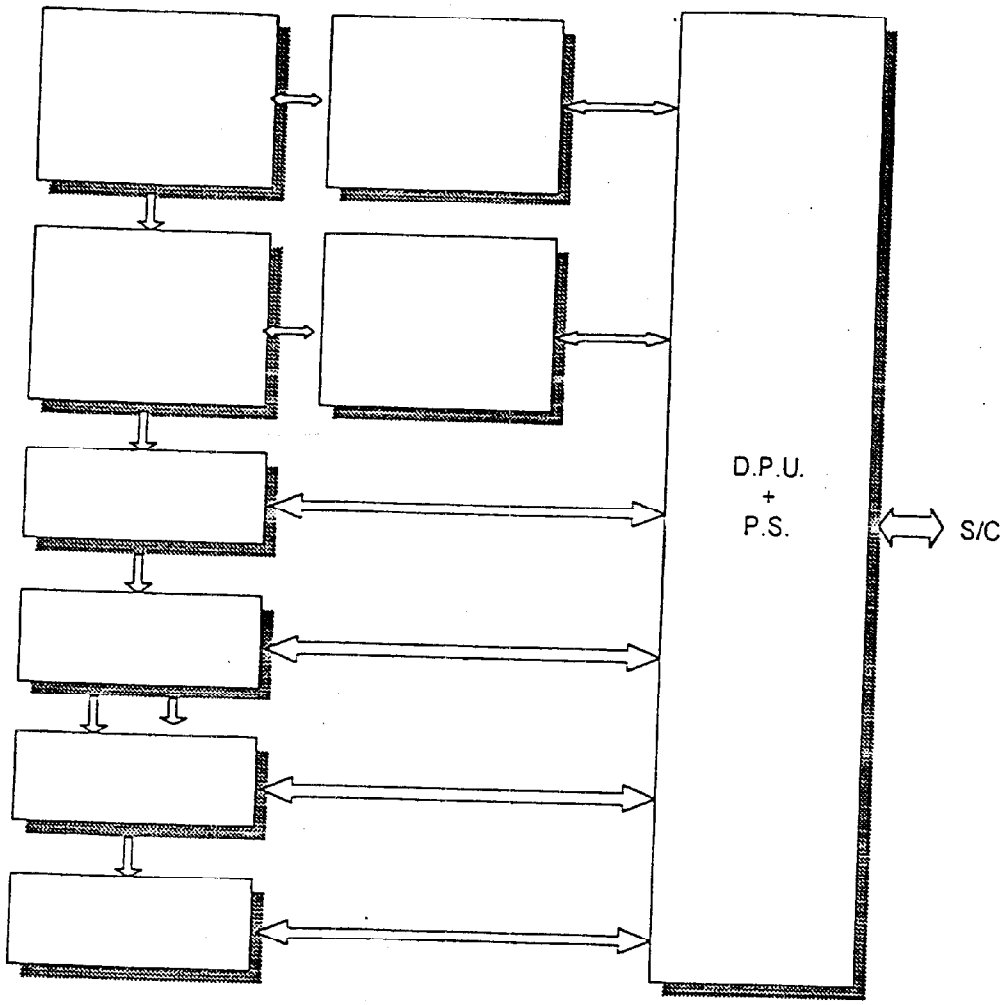
After that, the companies will be invited to formally place their orders, and a grouped procurement will be organised.

Conditions
The questionnaire aims at evaluating all HIREL and non HIREL needs regarding 31750, MMU and possibly EDAC, for ESA and non ESA-Programmes, with the exception of those HIREL parts quantities known as procured by Central Parts Procurement Agencies for ESA programmes (i.e. for XMM, INTEGRAL, ROSETTA, CLUSTER II, COF, ATV, METOP, Meteosat SG, FIRST and PLANCK).

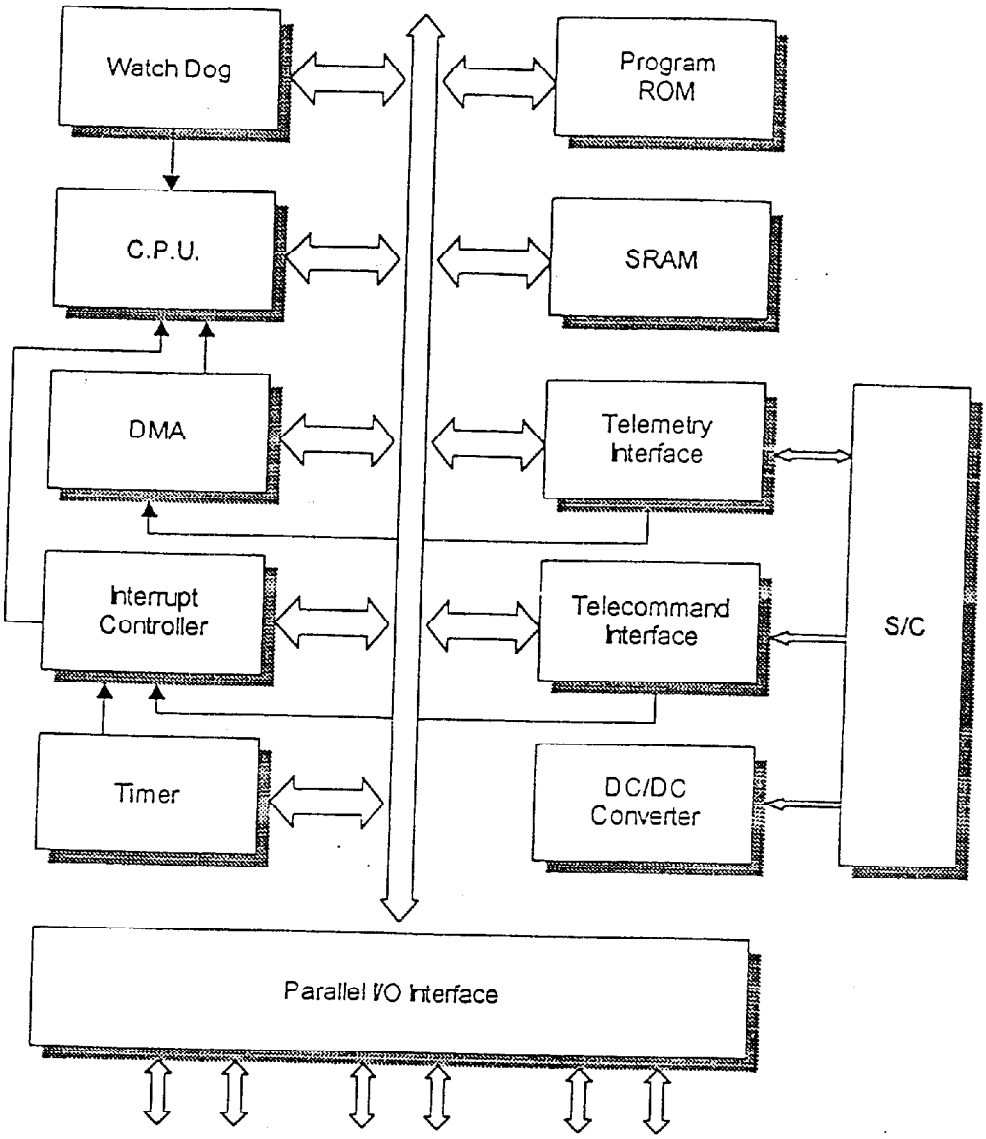
Questionnaire

1. What are the versions needed by your company?
2. What quality level
3. Please give your estimate of the quantity of parts needed versus quality level and version
4. Please indicate the need date.

Part 1.2.1.1.2	**Name:** QUESBDH.SE7 **Type:** unspecified type (application/octet-stream) **Encoding:** base64



PHOC Block Diagram



DPU Block Diagram

ISO SWS
FABRY PEROT

PROPOSED

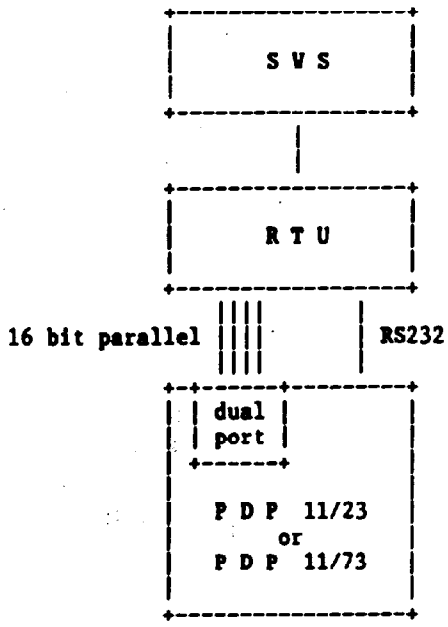
COMPUTER HARDWARE CONFIGURATIONS

FOR DIFFERENT CHECKOUT LEVELS

AND GROUND SEGMENT

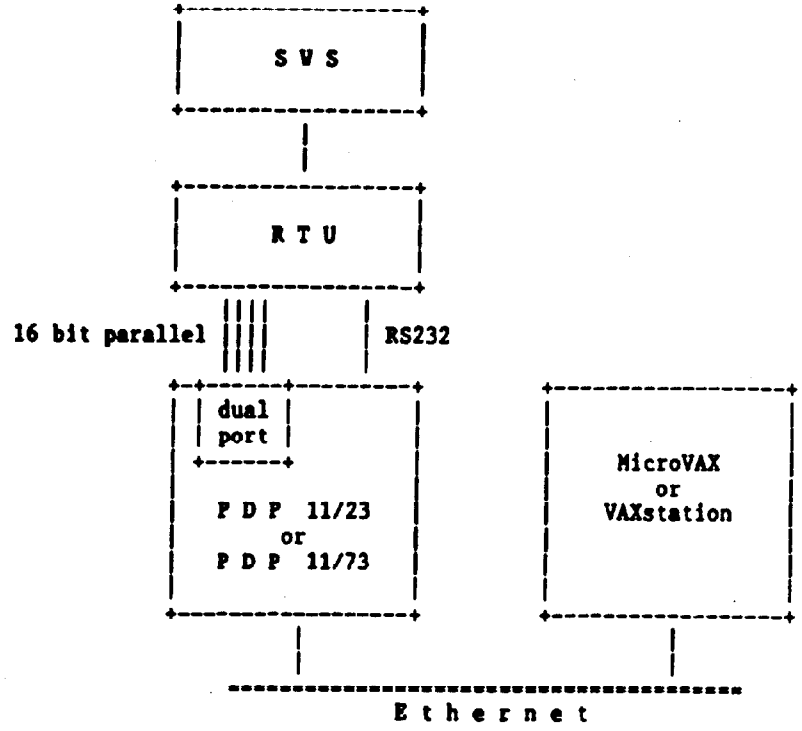
O.H. Bauer MPE-Garching

(1) Bench Level and lover Instrument Level

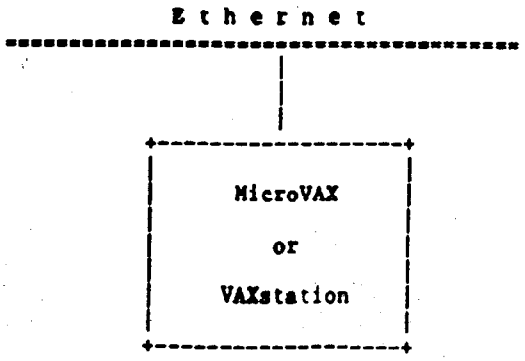


(2) Instrument Level

On Instrument Level the PDP 11/23(73) will be used as an intelligent interface for a MicroVAX or a VAXstation. The interface between the PDP and the VAX will be ETHERNET.



(3) Sstem Level Tests and Ground Segment



Mission Objectives	Far Infra Red Space Telescope, with ~~mechanically or~~ cryostat cooled instruments for observation in the submillimetre band
Operations Characteristics TBC	
Launch date	2007 → End 2005
Launch type	Ariane 5 GTO ~~multiple or~~ single launch
Operational lifetime	Nominal : 3 years (for costing) extendible up to 6 years 4.5y
Orbit Characteristics	Heliocentric, L2 halo
Earth distance	1.5 - 1.8 million km
Angle Sun - S/C - Earth	< 45°
Period	6 months (Halo)
Inclination	N/A
Observation Constraints	
Min. altitude	N/A
Sun Aspect Angle	60 - 120 deg (0 - 3 yr.) TBD 70 - 110 deg (4 - 6 yr.) TBD
Earth Aspect Angle	TBD
Eclipse operations	N/A
Attitude Control (95 % half cone)	
Absolute pointing error	8 arcsec
Relative pointing error	1 arcsec/min
Measurement accuracy	7 arcsec
Slew rate	> 7°/min
Max. slew angle	> 270°
Ground Segment Facilities	
LEOP Phase	S-band Perth (30m), Kourou, ESOC-MCR, Mission Dedicated Computer System (MDCS)
Routine Operations Phase	S-band Perth (30m). Kourou emergency back-up. or X-band ESOC-MOC, plus institutes (FSC,ICCs)

Table 1 - FIRST Mission Description

Autonomous operations (S/C + instruments)

- daily ground coverage : Kourou 11 hrs
  Perth 6 - 12 hrs
- command schedule loaded on-board (24 hrs
  - daily science operations 22 hrs (mass memory
  - daily telecommunications 2 hrs (TC + TM)

2.2 Spacecraft Characteristics : Heliocentric L2 halo

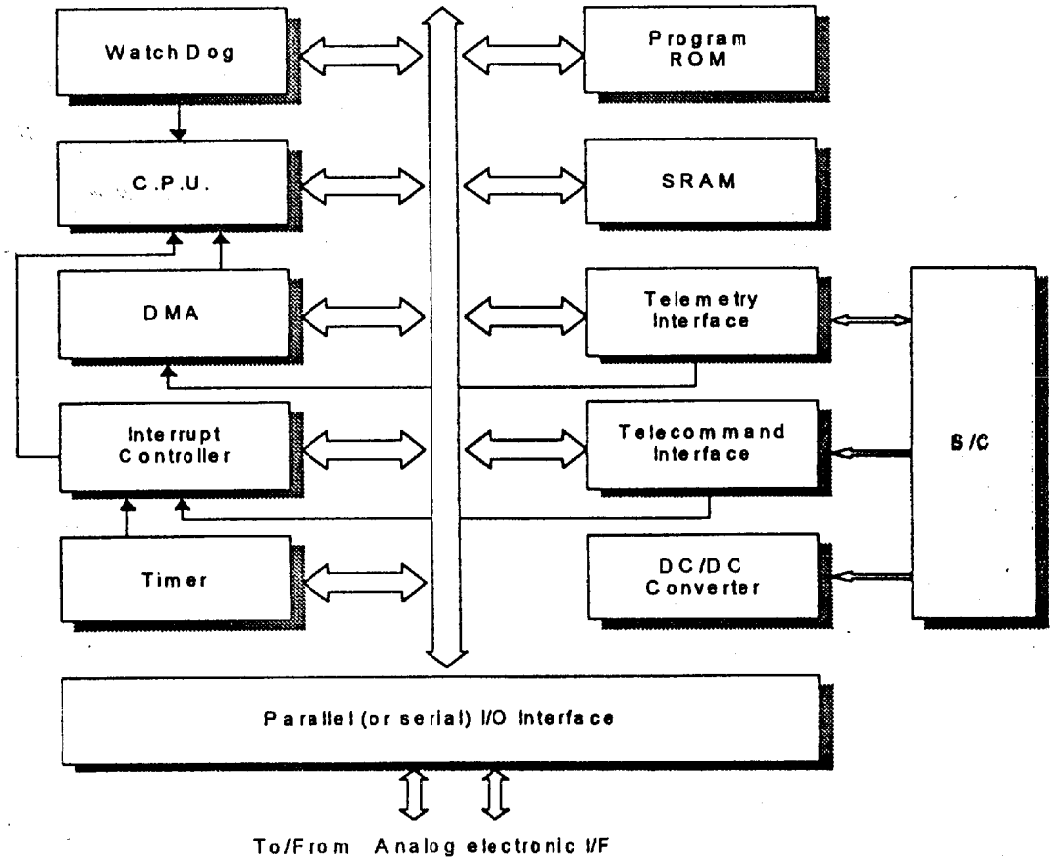
Diminsions	
Size	6.61 x 4.30 m
Launch Mass	4040 kg
Payload Mass	1295 kg
Propellant Mass	640 kg
Orbit and Attitude Control	
RCS	Monopropellant
Attitude Determination	Star Tracker, Sun Sensors, Gyros
Attitude Control	Reaction Wheels + Reaction Control System (momentum dumping)
Stabilisation	3-axes stabilised, APE 8, RPE 1 arcsec.
Observation Modes	Fine Pointing Raster Pointing Line Scanning Solar System Object Tracking Position Switching and Nodding
Power Generation	
Array architecture	Fixed arrays on cryostat sunshield
Array size	16 m²
Power consumption (max.)	805 w
Communications	
Frequency utilisation	S-band or X-band
TM Bit rate incl. OB Store transmission	Nominal dump : 243 Kbs plus coding or higher R/T HK : 2 Kbs R/T HK + Instrument : 42 Kbs
TC Bit rate	2 Kbs
Tx Power	5 w
Antenna gain	- 5.5 dBi (omni) + 15.5 dBi (High gain)
Modulation	TM : direct SPL (High BR) or PSK/PM (low BR) TC : PSK/PM
Coding	Reed Solomon + Convolutional
Thermal Control	
Paylod cooling method	He₃ cryogen
On-Board Data Handling	
Max. S/C Autonomy	> 72 hrs !!
Standards	Full Packet Telemetry
Mass Storage	TBD : 3.6 Gbit

IFSI is proposing to manufacture the 3 DPU for FIRST (1 for Planck as well).

This approach will force some kind of standardisation:

- uP general design and S/C I/F
- OBS: language, overall design, S/C I/F , documentation
- Similar APU I/F. Parallel or serial
- Save some money

DPU block diagram



APU Interfaces

As simple and general as possible in order to replicate for the 3(+1) instruments.

- Parallel I/F exporting data address and direction coded in a 8 or 16 bit word.
  - Easier to implement.
  - Fast
  - More wires
  - Difficult to duplicate (redundancy)
- Serial I/F exporting data address and direction coded in a 8 word.
  - Need some HW also on the APU side
  - Slower (e.g. 500 KHz clock)
  - few wires
  - easy to duplicate

Interface proposal

Serial

- 2 Serial 16 bit registers. Can be managed as for (old) ESA telemetry/telecommand standard
- Proposed clock frequency ~ 500KHz (~ 50 uS/word)
- Might foresee up to 8 bit parallel lines

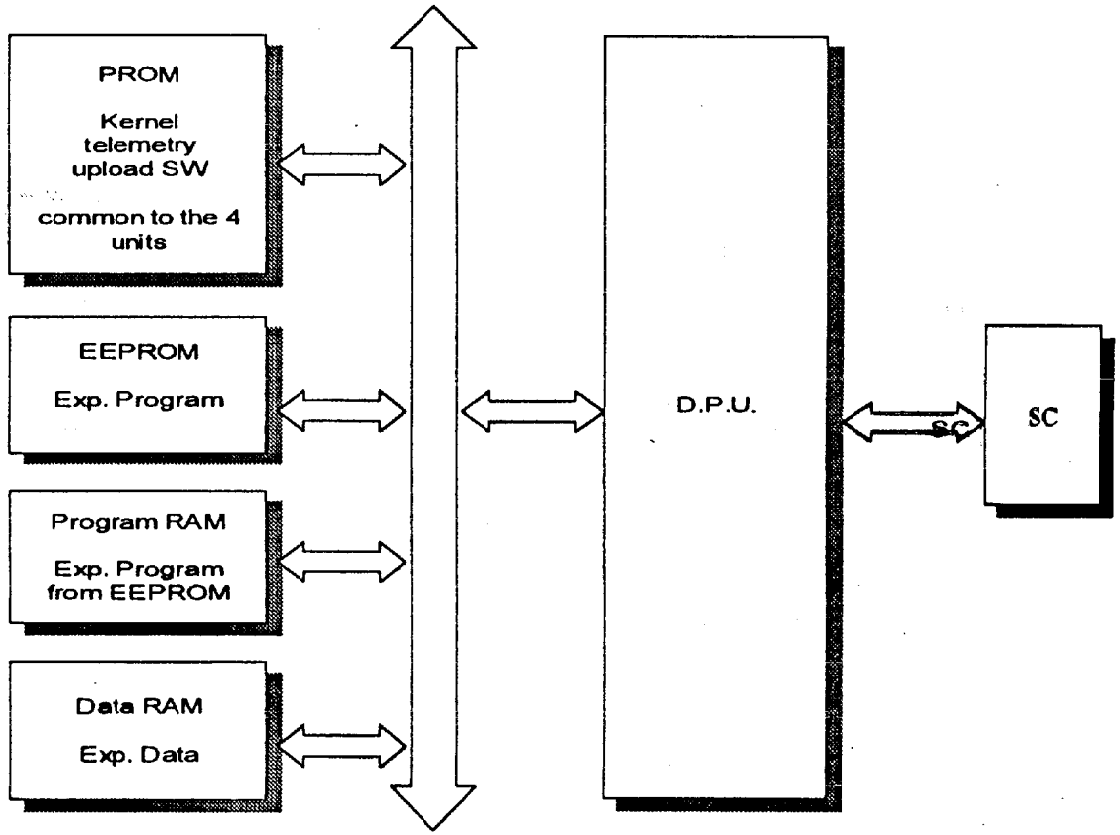
Parallel

- 16 bit parallel port(s) is the alternative to the serial one

On Board Software design

- Will use C language for main part of OBS (depends on uP family)
- Program stored in PROM and EEPROM, execute both in EEPROM and RAM
- Possibility to upload the instrument program with experiment integrated on S/C
- Upload patches and new parameters during mission
- Upload new instrument program during mission if enough upload telemetry is available

Memory organisation



uP Family

- We will push for Intel (AMD) 80C186.
- We might be "invited" to use the Marconi MA31750

Redundancy

- Depends on the allowed weight and volume.
- Plan to redound at board level (2 CPU+mem 2 APU I/F 2 DC/DC converter)
- Upload SW patches (or full program)

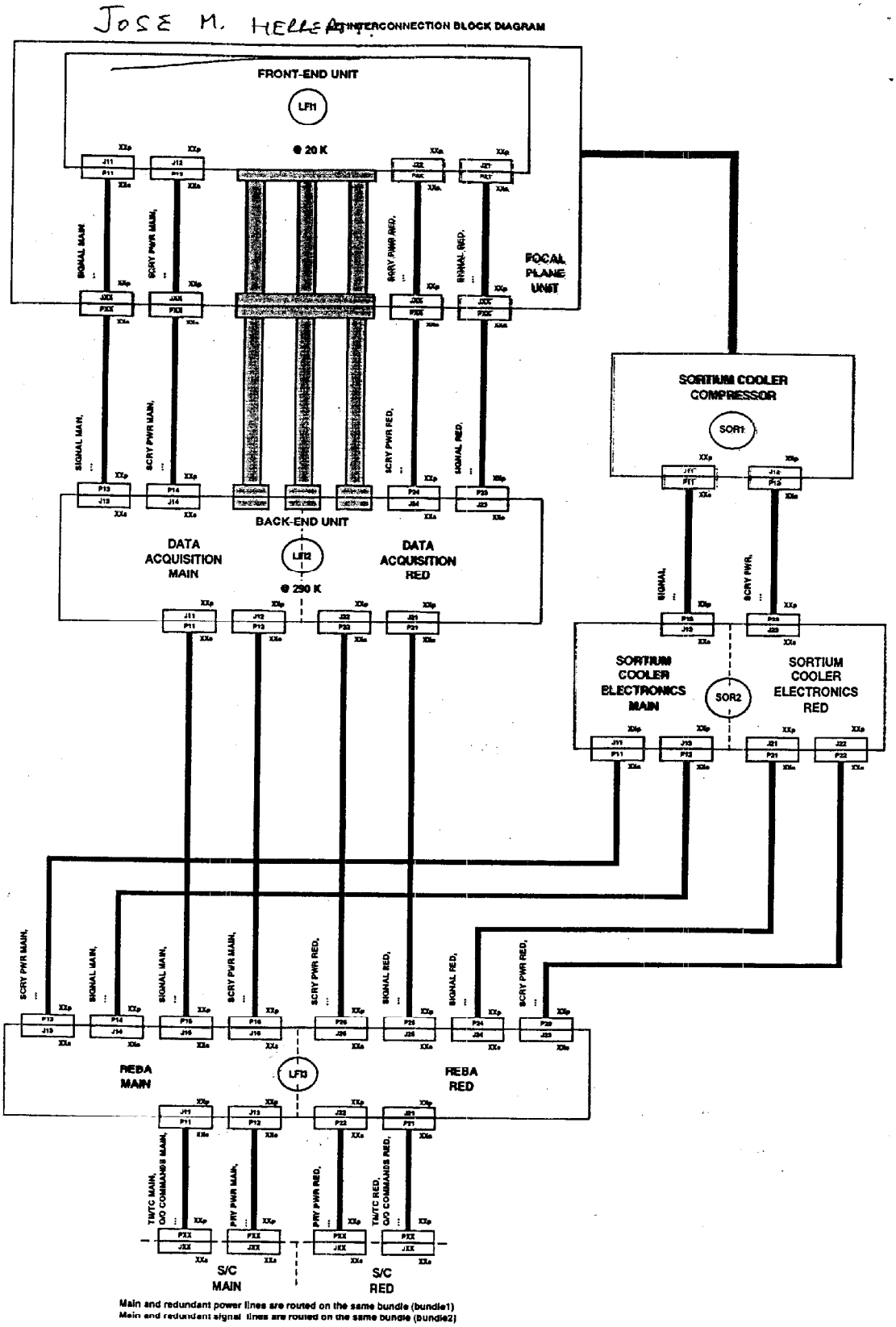
Test Philosophy

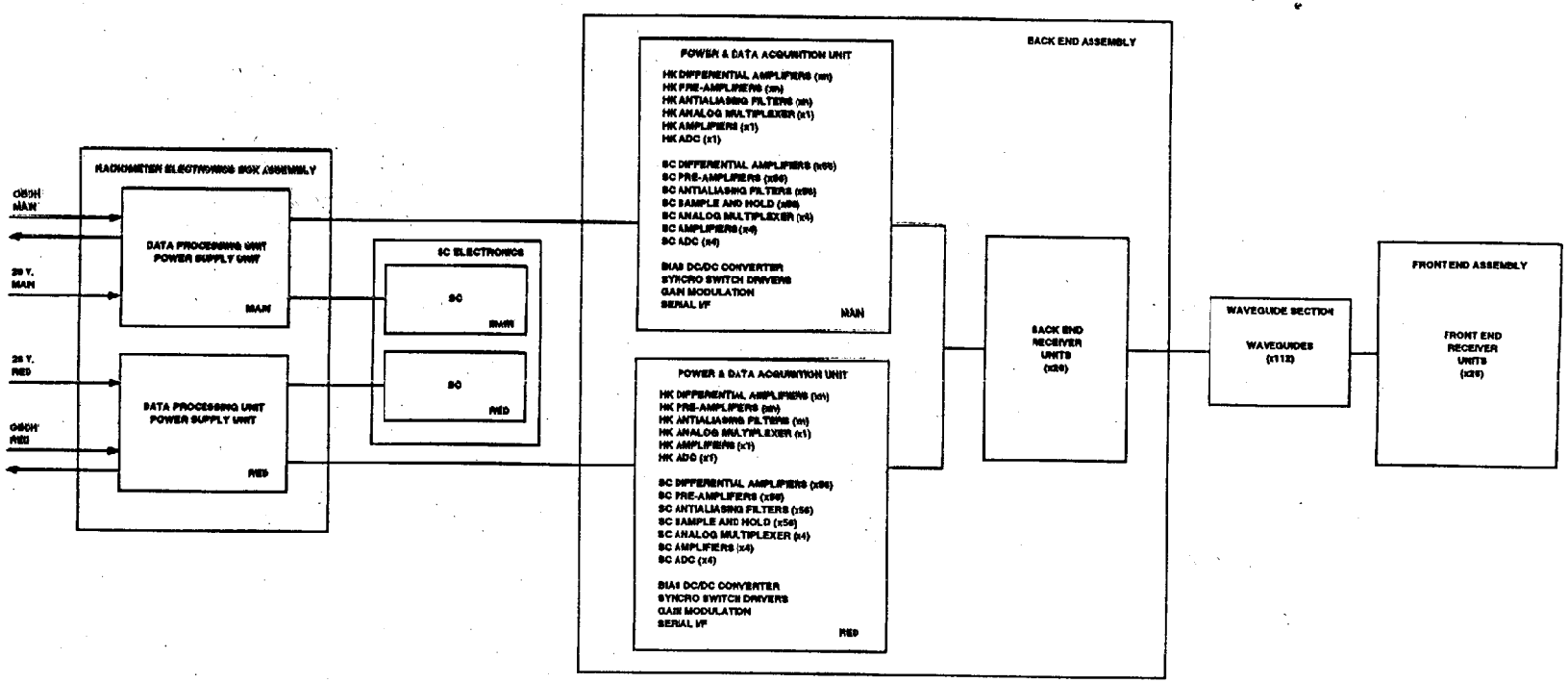
- We do not deliver any test HW
- Spacecraft simulator (PC board) for internal use can be designed in collaboration with experimenters and/or ESA
- EGSE should be ready for instrument level testing
- Availability of experiments simulators is appreciated
- EM like unit will be delivered to every exp. Institution

Physical resources

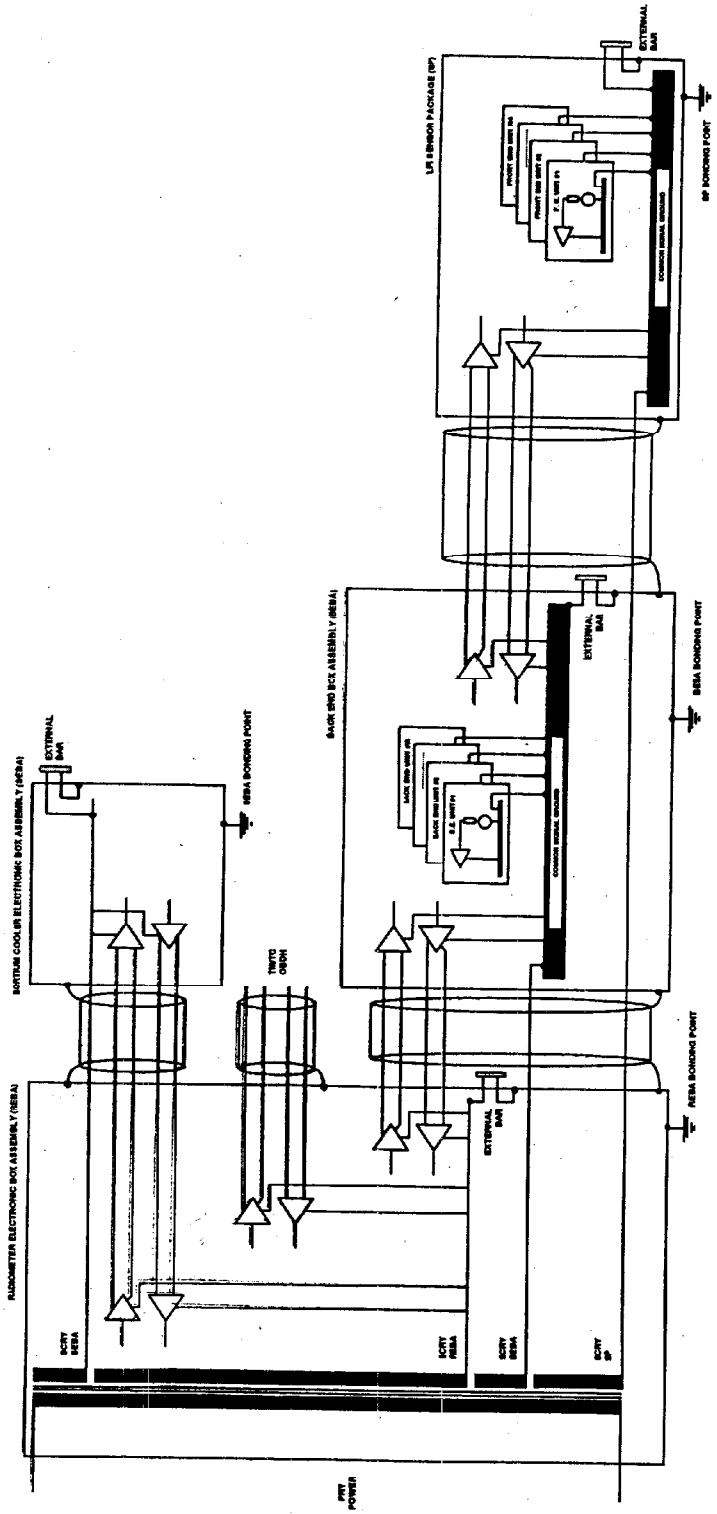
- Might foresee 5 Kg 5Liters 5Watt depending on board redundancy and overall power requirements
- Estimate cost is 10 Glira or 3.6 M pounds (salaries not included) for 4 units

JOSE M. HERLE


INTERCONNECTION BLOCK DIAGRAM
FRONT-END UNIT
LFI1
@ 20 K
FOCAL PLANE UNIT
SIGNAL MAIN
SCRY PWR MAIN
SCRY PWR RED
SIGNAL RED
SORTIUM COOLER COMPRESSOR
SOR1
BACK-END UNIT
DATA ACQUISITION MAIN
LFI2
@ 250 K
DATA ACQUISITION RED
SORTIUM COOLER ELECTRONICS MAIN
SOR2
SORTIUM COOLER ELECTRONICS RED
REBA MAIN
LFI3
REBA RED
TM/TC MAIN, O/O COMMANDS MAIN
PRY PWR MAIN
PRY PWR RED
TM/TC RED, O/O COMMANDS RED
S/C MAIN
S/C RED
Main and redundant power lines are routed on the same bundle (bundle1)
Main and redundant signal lines are routed on the same bundle (bundle2)



LFI REDUNDANCY CONCEPT


LFI GROUNDING SCHEME (MAIN)

COBRAS/SAMBA DATA HANDLING

Data Rates

Using July 1996 allocation of channels:

Freq	30	44	65	100	Ghz
No of channels	4	4	18	30	
Angular resolution	30	21	14	10	arcmin
Beam crossing time [1]	89	62	41	30	ms
Sample time [2]	36	25	17	12	ms
Samples / Spin period	1650	2358	3538	4952	
Total rate [3]	1.8	2.5	17.0	39.6	kbps

Notes:
1. Assuming spin rate = 1 rpm and LOS at 70° to spin axis.
2. Oversampling factor 2.44 ($t_{samp} = t_{cross} / 2.44$)
3. Assuming 16 bit readout for all channels.

$\therefore$ Total TM Rate $\approx$ 60.9 kbps $\Rightarrow$ 62 kbps (incl. H/K)

This is similar to Red Book value (somewhat lower)

Assume
- Downlinked TM data rate = 60 kbps (total)
- 1/3 allocated to LFI
- Ground contacts 10 hr/day (min)

Mean data rate available for LFI $\approx$ 8.3 kbps

Compression factor required $\approx$ 7.4

LFI Data Processing Unit

System architecture: based on the MIL-STD-1750 architecture

On-board microprocessor:
MA31750 (see CRISA's email)
PACE1750

On-board programming language: "C"

Digital Serial I/F: "RS-422"

Processing Module: (tbc)

Dedicated DSP processor to perform the data compression with the following characteristics:
TSC21020E processor architecture running at 13 MHz (tbc)
64K (tbc) x 32 Ram for Data Storage
32K x 48 RAM for Program Storage
8K x 48 Boot PROM

Lose-less Compression Algorithm : Rice (tbc)

Instituto de Astrofísica de Canarias (IAC)

The IAC Participation in FIRST/Planck

Planck:

LFI

First:

PHOC
BOL

Key Personnel

Rafael Rebolo - LFI CO-I
Jordi Cepa - PHOC Co-I
Ismael Pérez - BOL Co-I
José M. Herreros - Local Project Manager

Possible Areas of Participation (I)

LFI:

- On-board digital electronics - Command and Data Handling System.
- On-board analogue electronics.
- On-board power electronics.
- On-board software.

Implementation Plan

- System Electronic Specifications - IAC, LFI Consortium and CRISA. (In progress)
- On-board Software:
  Architectural design, detailed design, coding and test. IAC
- Digital, analogue and power electronics.
  Conceptual design. IAC, LFI Consortium and CRISA. (In progress)
  Detailed design and manufacturing. Industry
  Functional test. Industry
- Boxes.
  Mechanical design. IAC and Industry
  Manufacturing. IAC
- Environmental test. Spanish National Space Agency -INTA.

Possible Areas of Participation (II)

PHOC:

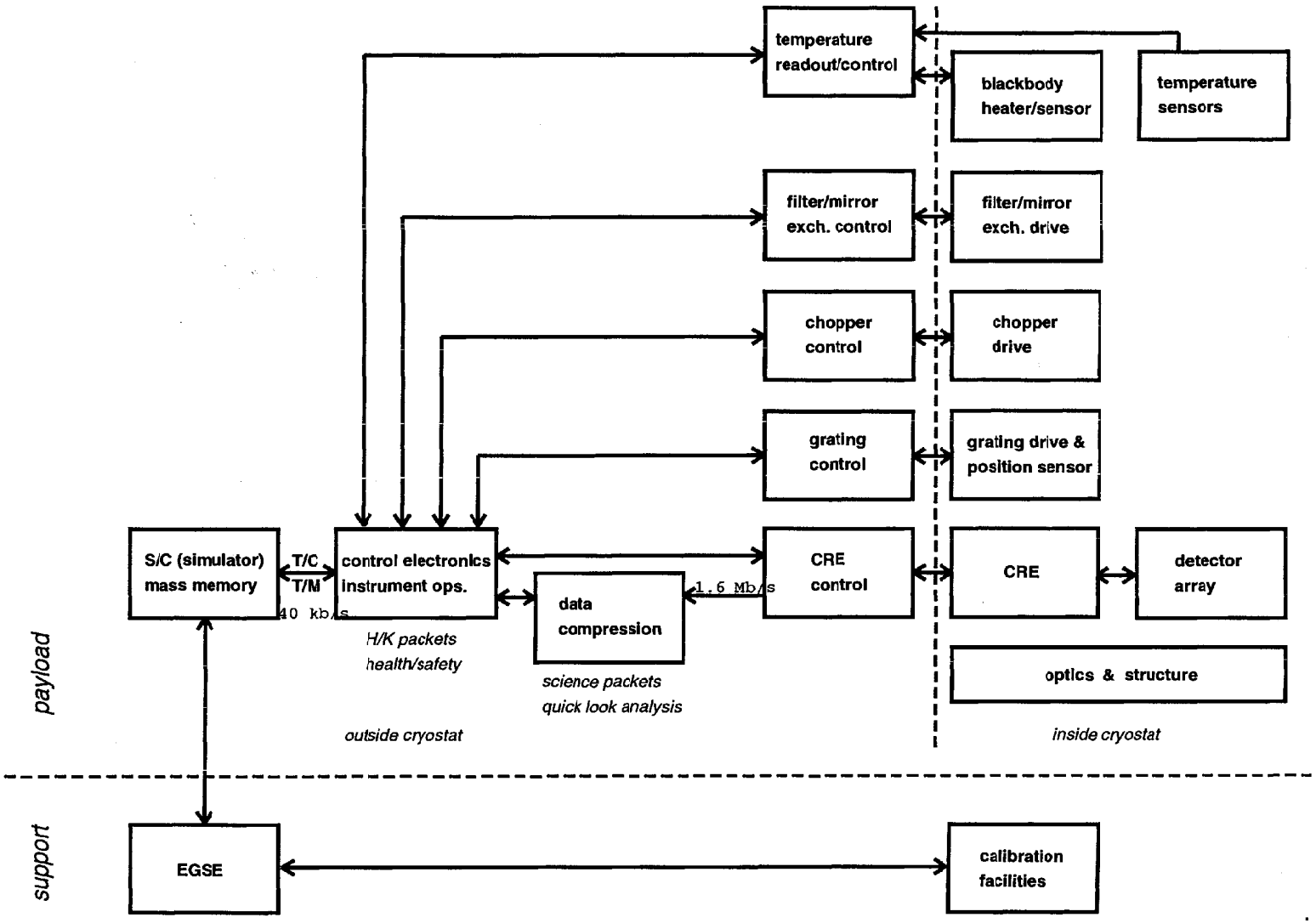
Data Compression Unit. HW

- Unit Specification. IAC and PHOC Consortium
- Design and manufacturing. Industry
- Environmental test. Spanish National Space Agency -INTA.
- Boxes.
  Mechanical design. IAC and Industry
  Manufacturing. IAC

BOL:

It is being defined.
Interest on digital electronics.

PHOC Configuration Scheme

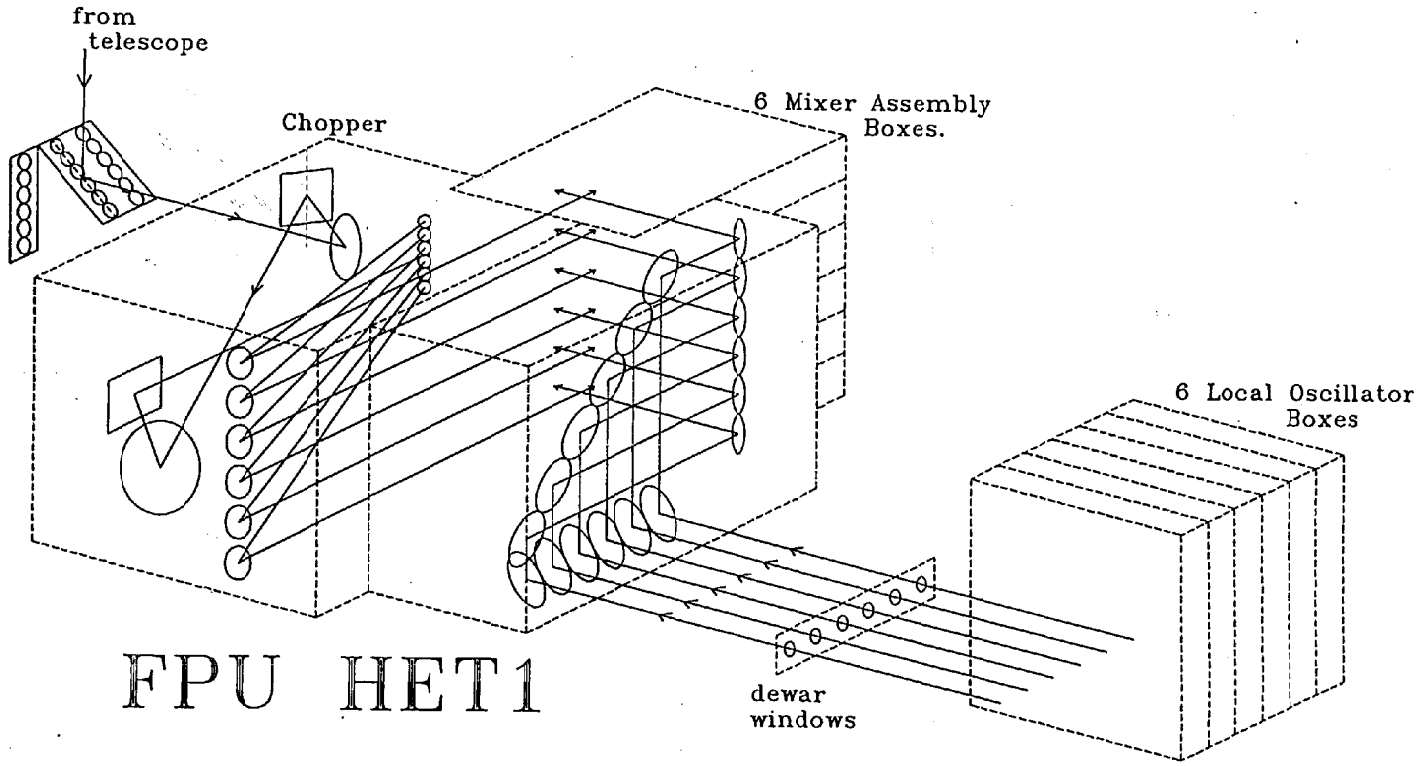


DPU Data Rate/Interface Requirements for PHC

	Input	Output
Temperature Readout/Control	**Target Temperatures for BBs** 2 x 16 bit, 0.1/s	**Actual Temperatures in PHC** 10 x 16 bit, 0.1/s
Filter/Mirror exchangers control	**Target Positions** 1 x 16 bit , 0.1/s	**Actual Positions of Mechanisms** 1 x 16 bit , 0.1/s
Chopper Control Alternative I ("Intelligent" Controller)	**Chopper Control Words (Throw, Offset, Waveform)** 10 x 16 bit, 1/min **Update Chopper Params** 2 kB, 1/day **Sync Ref** 1 bit, <= 10/s	**Chopper Status** 10 x 16 bit, 1/min **Sync/On Target** 1 bit, <= 10/s
Chopper Control Alternative II ("Dumb" Controller)	**Chopper Position Words** 16 bit , 2000/s **Update Chopper Params** 2 kB, 1/day	**Sync/On Target** 1 bit, <= 10/s
Grating Control	**Grating Target Position Word** 16 bit, <= 10/s	**Grating Actual Position Word** 16 bit, <= 10/s
CRE Control	**CRE Params (Bias, Integration ...)** 64 x 16 bit, 1/min **Sync Ref** 1 bit, <= 10/s	**CRE Status** 64 x 16 bit, 1/min
Data Compression Unit	**CRE Params (Bias, Integration ...)** 64 x 16 bit, 1/min **Sync Ref** 1 bit, <= 10/s **Compression Commands** 64 x 16 bit, 1/min **Algorithm Update** 1 hr Max Uplink Rate, 1/week	**DATA** 40 kbit/s

HIFI Schematic Diagram

2 Nov '97.



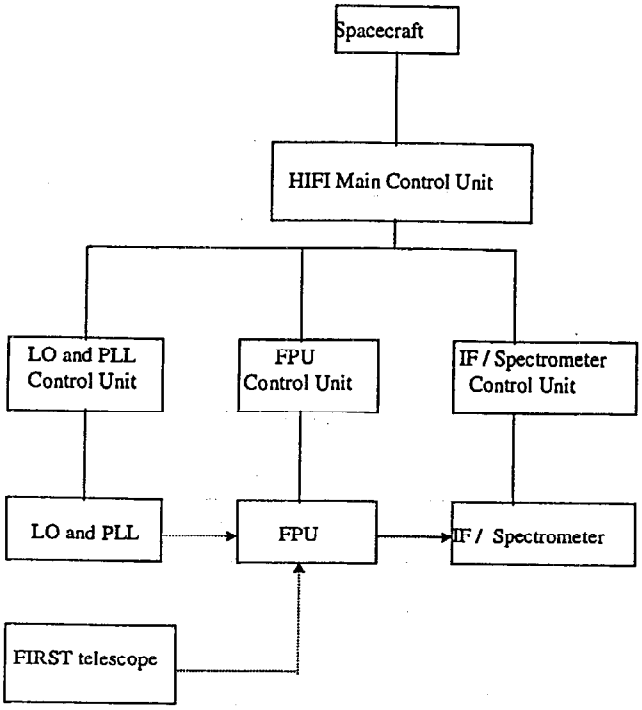
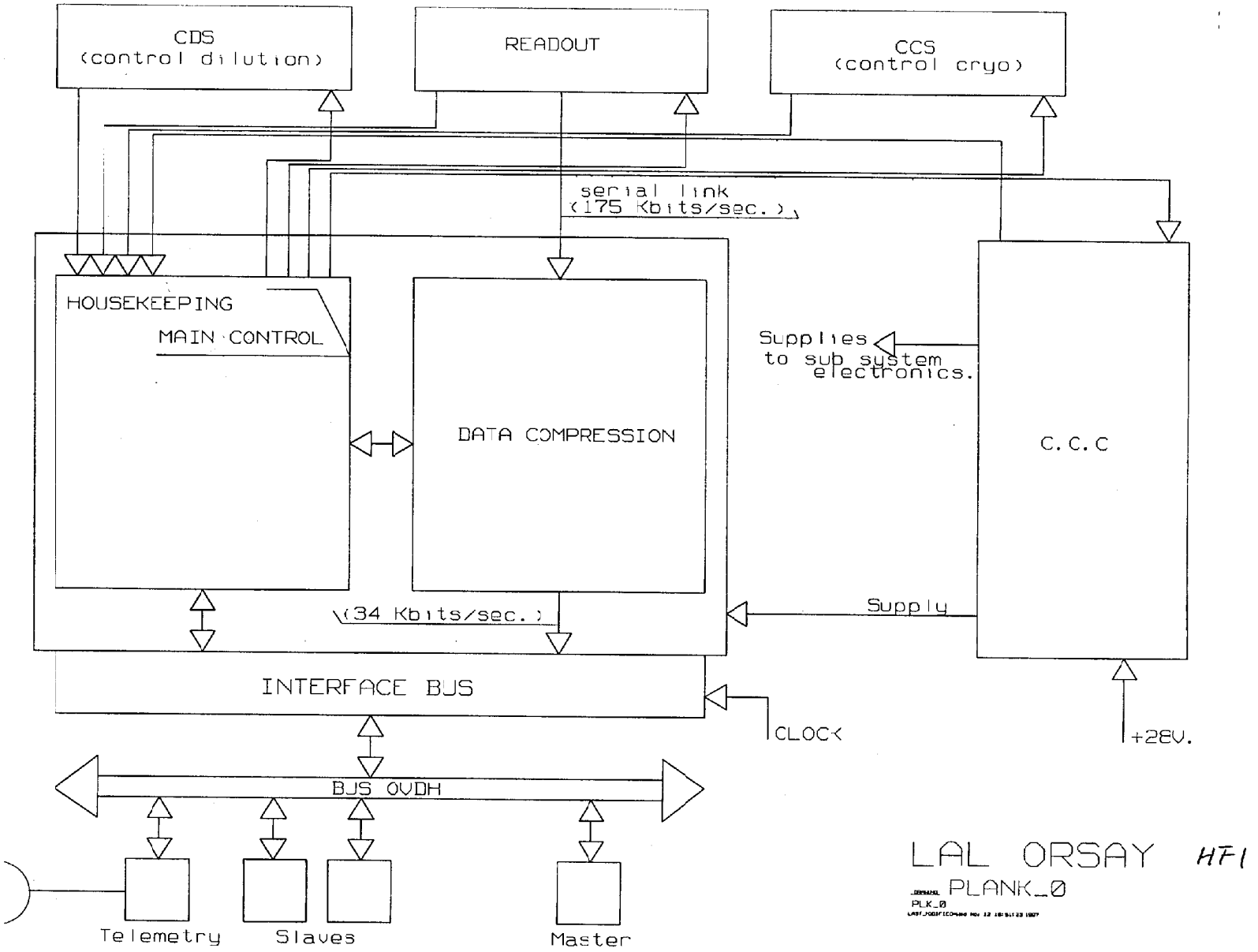


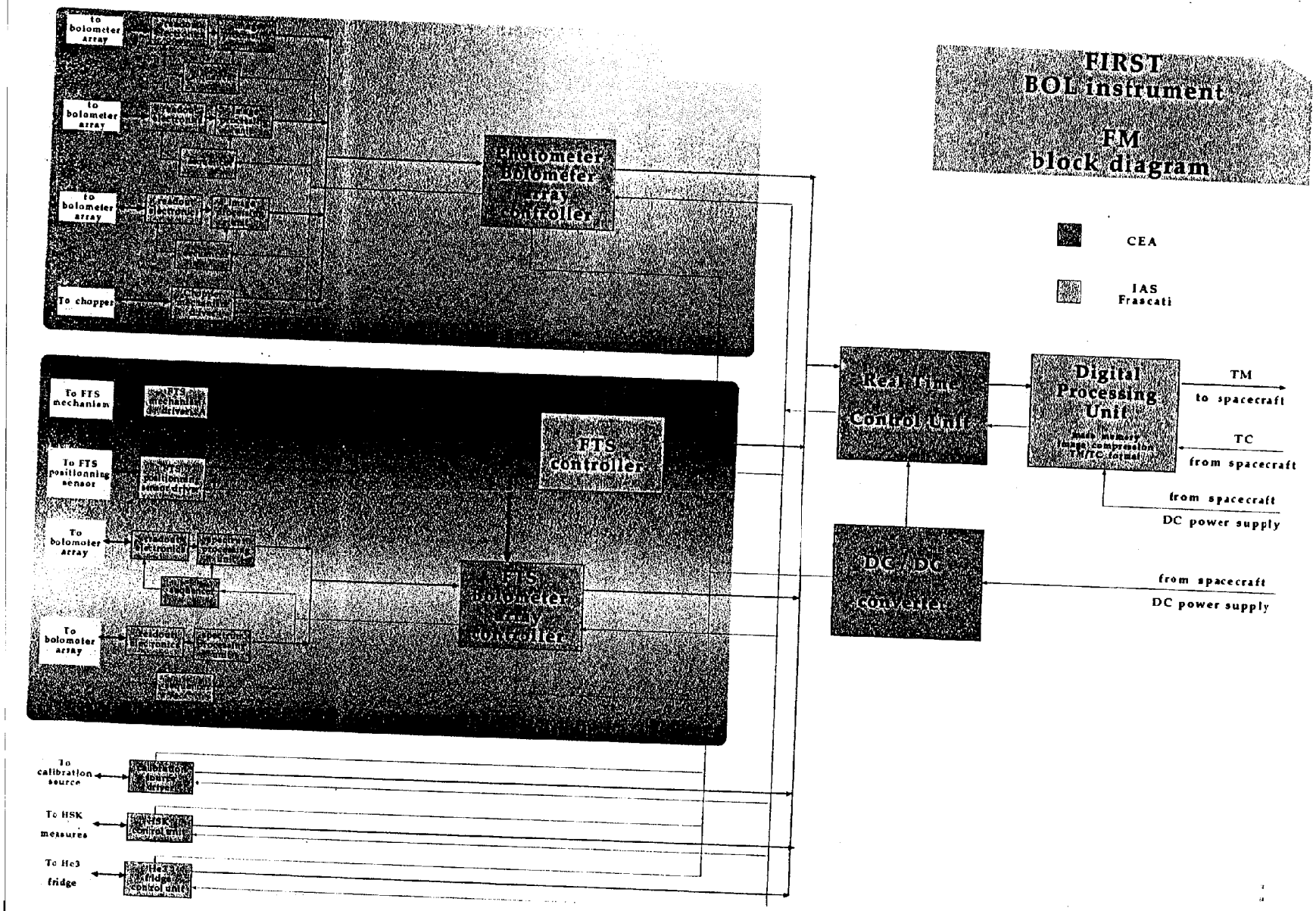
Fig. 1. The HIFI instrument in the flight configuration. Shown are the control and power interfaces, plus the signal interfaces between the subsystems.

It is assumed here that the mixer assemblies are incorporated in the FPU subsystem and that the IF system is separate.

HIFI Particularities

- Expected to be prime for full 24-hour periods
- Expected to need the full uplink and downlink capacities
- Expected to use all pointing modes
- Synchronization with S/C (OTF, … ?)
- Has 12 virtual apertures
- Diffraction-limited downto 120 μm
- Needs autonomous routines to optimize settings and to condition the system
- Data format will depend on back-end configuration


CDS
(control dilution)
READOUT
CCS
(control cryo)
serial link
(175 Kbits/sec.)
HOUSEKEEPING
MAIN CONTROL
DATA COMPRESSION
Supplies
to sub system
electronics.
C.C.C
(34 Kbits/sec.)
Supply
INTERFACE BUS
CLOCK
+28V.
BUS OVDH
Telemetry
Slaves
Master
LAL ORSAY HFI
PLANK_0


FIRST
BOL instrument
FM
block diagram
CEA
IAS
Frascati
to bolometer array
to bolometer array
to bolometer array
To chopper
Photometer Bolometer array controller
To FTS mechanism
To FTS positionning sensor
To bolometer array
To bolometer array
FTS controller
FTS Bolometer array controller
To calibration source
To HSK measures
To He3 fridge
Real time Control Unit
Digital Processing Unit
TM
to spacecraft
TC
from spacecraft
from spacecraft
DC power supply
DC / DC converter
from spacecraft
DC power supply

GNU-Based Compilation Systems for Spacecraft Microprocessors

M. Martignano, Mathematics and Software Division, ESTEC

❒ Résumé

L'article présente les activités en cours et en projet à l'Agence en vue de mettre au point des systèmes de compilation fiables et peu coûteux pour microprocesseurs de bord. On précise les impératifs auxquels doit répondre un tel système et les caractéristiques qu'il doit offrir. On examine à titre de point de départ un système à base d'outils GNU. On décrit enfin l'état d'avancement actuel des travaux et les projets en la matière.

❒ Contractors:

Chris Nettleton Software (UK)

❒ Budget:

General Infrastructure Budget

❒ Introduction

The European Space Agency has a comprehensive policy for the choice and procurement of on-board microprocessors. For 16-bit applications, microprocessors which meet the American standard MIL-STD-1750A (and 1750B) are recommended; for 32 bit applications, the SPARC V7 architecture is preferred. ESA has developed hardware which meets both specifications. (*Preparing for the Future* Vol. 3 No. 2 and Vol. 5 No. 1).

The success of a computer procurement policy depends on the availability of appropriate tools which satisfy the specific needs of developing software for spacecraft. One of these essential tools is a compiler which (put simply) translates the code written by the programmer into the machine language instructions which drive the computer. The long duration of space projects, requires that compiler systems be stable and that they be supported for ten years or more to guarantee post-launch maintenance of flight software. They must also be inexpensive, and attractive to payload developers in research institutes.

A microprocessor procurement policy must have a corresponding software policy; but due to the large number of programming languages available, only a limited number of these can be supported. For the short term, only the C language (conforming to ANSI/ISO 9899) and Ada-83 language (ANSI/MIL 1815A) will be supported. It is intended that C++ and Ada-95 (ISO/IEC 9638) languages may be added, once their maturity has been established.

ESA has followed with considerable interest the work done in the USA by the Free Software Foundation in developing the GNU C Compiler [1] and by New York University in developing an Ada-95 translator. The use of these compilers is being promoted by ESA as a way of obtaining reliable low-cost compilation systems for spacecraft microprocessors.

❒ Compilation systems

To develop software applications in a given language for a particular target processor, a compiler alone is not enough. Other tools such as a 'linker' and a 'library archiver' are needed to generate executable images. The use of existing libraries of executable routines, which may be called by the program during its execution avoids having to 'reinvent the wheel' through rewriting unnecessary code during development of an application. The compiled application program may run on the bare hardware or above a small real time executive or real time operating system.

The term 'compilation system' covers the set of tools and libraries mentioned above:

- the compiler;
- the language run-time support, which allows the language virtual machine to execute;
- binary utilities such as the assembler, the linker, the library archiver;
- a library (or set of libraries) containing routines, functions often used when writing application;
- a tool for detecting and correcting programming faults (a debugger);
- an integrated development environment, a graphical user interface which allows the user to edit source files, and to easily activate all the other tools of the compilation system.

Although it is preferable to develop software by running it on the computer for which it was written, it sometimes happens that the target computer is not available or is inconvenient to use. In these cases, it is usual to develop software on another computer

which has been programmed to simulate the target computer. In addition, the following tools and libraries could the be included in a compiler intended for writing space software applications:

- one or more real time executives (small operating systems) to provide the application developers with an already developed (and working, and tested) multitasking system;
- a library (or set of libraries) providing services often used in space applications such as telemetry and telecommand, services and collection of satellite housekeeping data.

❒ The GCC and GNAT compilers

GCC is a C/C++ compiler which was created in the context of the Free Software Foundation's GNU activities. GNAT (GNU New York University Ada Translator) is an Ada-95 front-end for the GCC compiler. The main advantages of these compilers are:

- they are both freely distributed;
- they have a large and active user communities, which compensates for the lack of conventional support and maintenance;
- errors in are widely reported and remedies and/or work-around solutions are published by the same users;
- they require a minimum of computer resources (RAM memory, hard disk space);
- their quality (e.g. the quality of their front-ends) and the quality of the generated code (size and performance) is good, and compares well with commercial products.

Let us now take a look at available products and some plans for the future.

❒ MIL-STD-1750A/B compilation system

This compilation system supports the MIL-STD-1750 architecture. It is composed of a set of tools developed by Chris Nettleton Software:

- GNU C compiler ;
- Linker, assembler, archiver;
- standalone C library;
- Posix-Threads library, a pre-emptive real time executive which meets the portable operating system interface defined by the IEEE [2];
- GNU debugger with 1750 assembler;
- graphical user interface for the GNU debugger.

Binary versions are available and these run on under the Solaris-2.5, Linux-2.0 and Windows 95/NT operating systems.

❒ SPARC V7 compilation system

ERC32 is a microcomputer system, developed by ESA, to meet the requirements of the SPARC V7 architecture A cross-compilation system for this processor comprises:

- a GNU C and C++ compiler; a linker, assembler and archiver stand-alone C-library;
- GNU C++ libraries (libg++ and libstdc++)
- RTEMS, a real-time executive for multiprocessor systems kernel with support for the ERC32 microprocessor;
- a programable read-only memory utility for starting up the ERC32;
- a standalone ERC32 simulator; GNU debugger with ERC32 simulator)
- graphical user interface for the GNU debugger.

Binary versions of this cross compilation system which run under the Sunos-4.1.3, Solaris-2.5, Linux-2.0 and Windows-95 operating systems are available.

❒ Useful extensions

The following useful extensions could be added to both compilation systems:
saturated arithmetic, which avoids problems with exceptions arising out of numerical overflow and underflow,
user-definable criteria for handling exceptions, for example, an application will continue to run even after an exception has occurred;
user services such as a set of libraries of telemetry, telecommand and housekeeping routines;
a test coverage tool.

❒ Conclusions

The use of GCC and GNAT has proved to be an excellent and viable starting point for developing inexpensive compilation systems for microprocessors with the MIL-STD-1750 and the SPARC V7 architectures. The compilation systems will be accompanied by a set of high-level tools and libraries that will facilitate the development of software applications for space.

To provide a service to industry and research institutes in the European space community, a software distribution infrastructure and a repository for compilation systems, with appropriate long-term support, will be set up.

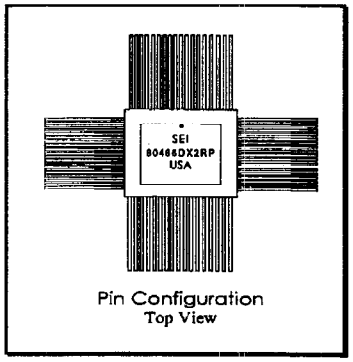
❒ References

[1]. GNU - a recursive acronym for "GNU is not Unix"; Unix is a family of operating systems, the first one was developed by AT&T.

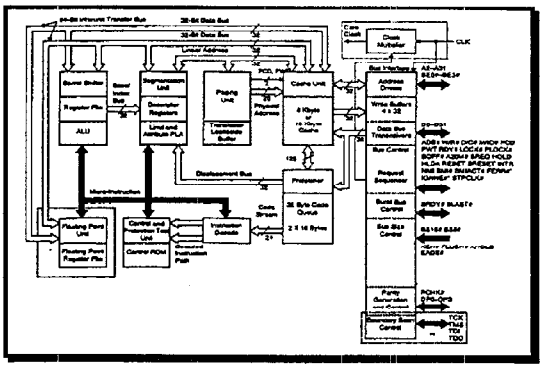
[2] IEEE 1003.1c-1995, defined by the I.E.E.E, New York, USA. ●

SEi - Radiation Hardened 80486DXRP

32-Bit Microprocessor



Pin Configuration
Top View



Features:

- 32-Bit Microprocessor
- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness >100 Krad (Si)
- Single Event Effect
  - SEL_{TH} = 59.6 MeV/mg/cm²
  - SEU_{TH} = 5 MeV/mg/cm²
- Package:
  - 208 Pin RAD-PAK® Quad Flat Pack
- 8 Kilobyte On-Chip Cache with Consistency Support
- External Cache Control
- Integrated Floating-Point Unit
- Single Cycle Execution
- 32-Bit RISC Integer Core
- Instruction Pipelining
- On-Chip Management Unit
- Write Buffers
- Bus Backoff
- Instruction Restart

SEi's 80486DX2RP (RP for RAD-PAK®) high performance 32-bit microprocessor features a typical 100krad (Si) total dose tolerance. The 80486DX2RP processor integrates an 8K unified cache and floating-point (FPU) hardware on chip. The on-chip memory management unit is completely compatible with the 80386 processor. The on-chip cache memory allows frequently used data and code to be stored on-chip reducing accesses to the external bus. Its speed-multiplying technology, allowing the processor to operate at frequencies higher than the external memory bus. The clock multiplier on the 80486DX2RP improves execution performance without increasing board design complexity. It enhances all operating operation out of the cache and/or not blocked by external bus accesses. The burst bus feature enables fast cache fills. The patented radiation hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It provides a 100 Krad or better (Si) total dose survivability, based on a GEO type orbit. Actual TID tolerance is dependent upon orbit and mission duration. Capable of surviving in space environment, the 80486DX2RP is ideal for satellite, spacecraft, and space prove missions. It is available in Class S packaging and screening.

Contact SEi for full data-sheet.

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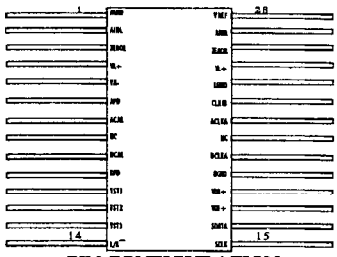
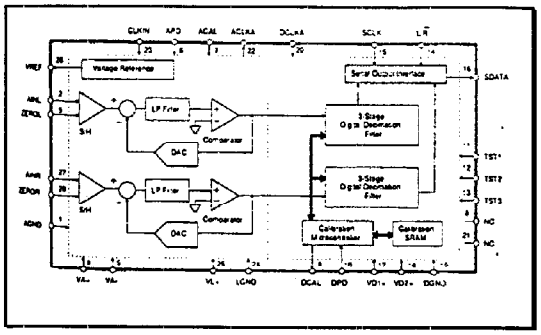
SEi - Radiation Hardened 5327RP

16-bit Analog to Digital Converter



PIN CONFIGURATION

TOP VIEW



Features:

- RAD-PAK® Radiation Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- Excellent Single Event Specifications
  - No Single Event Latchup
- Package:
  - 28 Pin RAD-PAK® flat pack (550 mils x 800 mils)
  - Weight – 6.0 grams
  - 28 Pin RAD-PAK® DIP (600 mils x 1400 mils)
  - Weight - 5.2 grams
- Low Power Technology
  - 450 mW Typical
  - 20 mW Power Down Mode
- 16-Bit Configuration
- CMOS 16 bit A/D Converter
  - On-Chip Voltage Reference
  - Internal 64X Oversampling
  - Serial Output
  - Two Input Channels
- True 16-Bit Precision
  - Low Noise: 95 dB Dynamic Range
  - No Missing Codes
  - S/(N+D): 92.7 dB Typical
  - THD: 0.0015%
- Screening per TM 5004
- QCI per TM5005

SEI's 5327RP (RP for RAD-PAK®) high resolution, high speed microcircuit features a minimum of 100 kilorad (Si) total dose tolerance. Fully equivalent to the commercial 5327, the 5327RP combines Crystal Semiconductor's advanced integrated circuit process and SEI's radiation hardened RAD-PAK® packaging. The 5327RP uses delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter. It performs sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16-bit values for both left and right inputs in serial form. The 5327RP is capable of operational sampling rates of up to 50 kHz per channel. It is also capable to achieve a dynamic range of 95 dB. Capable of surviving in space environments, the 5327RP is ideal for satellite, spacecraft, and space probe missions. The patented radiation hardened RAD-PAK® technology incorporates radiation shielding in the package. This product is available in Class S packaging and screening.

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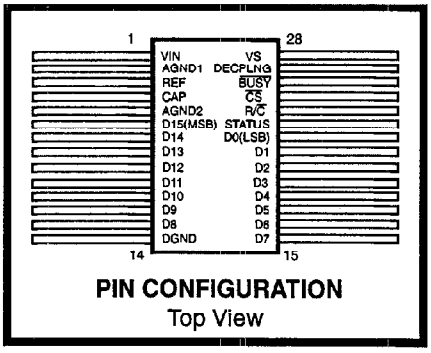
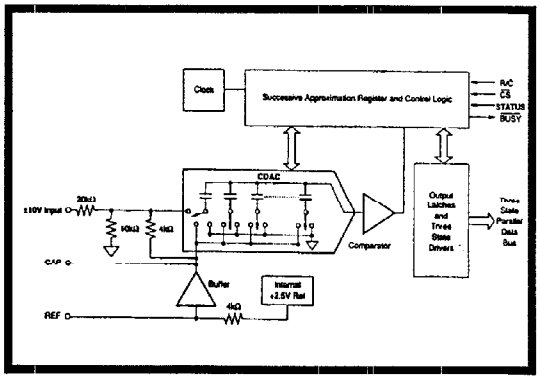
SEi - Radiation Hardened 7805ALPRP

16-Bit Latchup Protected Analog-to-Digital Converter



PIN CONFIGURATION
Top View



Features

- 16 Bit Organization
- Burr-Brown ADS7805 Core
- RAD-PAK® Technology Hardened Against Natural Space Radiation
- Latchup Protection Technology (LPT™)
- Package:
  - 28 Pin RAD-PAK® Flat Pack
  - 28 Pin RAD-PAK® DIP
- 100kHz min Sampling Rate
- Standard +10V Input Range
- Advance CMOS Technology
  - 86dB min SINAD with 45kHz Input
  - Single +5V Supply Operation
  - Utilizes Internal or External Reference
  - Full Parallel Data Output
  - Power Dissipation:
    132 mW Max
- Screening per TM5004
- QCI per TM5005

SEi's 7805ALPRP (RP for RAD-PAK®) high speed analog to digital converter features a minimum of 100 kilorad (Si) total dose tolerance. Using SEi's radiation hardened RAD-PAK® packaging technology, the 7805ALPRP incorporates the commercial ADS7805 from Burr-Brown. This device is latchup protected by Space Electronics LPT™ technology. It is a 28-pin, 16-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit capacitor-based SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers. The 7805ALPRP is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser trimmed scaling resistors provide an industry standard ±10V input range, while the innovative design allows operation from a single +5V supply, with power dissipation of under 132mW. The patented radiation hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It provides a 100krad or better(Si) total dose survivability, based on a GEO type orbit (actual TID tolerance is dependent of orbit and mission duration). Capable of surviving in space environments, the 7805ALPRP is ideal for satellite, spacecraft, and space probe missions.

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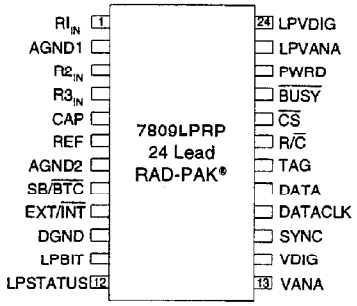
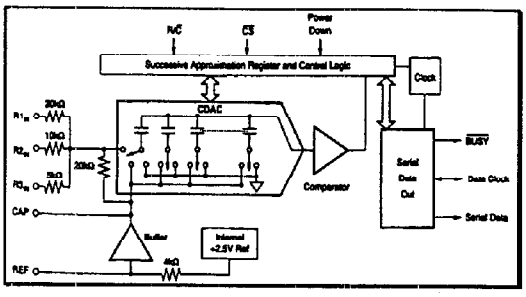
SEi - Radiation Hardened **7809LPRP**

16-bit Latchup Protected Analog-to-Digital Converter





Features:

- 16-Bit Organization
- RAD-PAK® Technology Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- Latch-up Protection Technology (LPT™)
- Same Footprint as ADS7809
- Package: 24 Pin RAD-PAK® Flat Package
- 100 kHz min Sampling Rate
- ±10V and 0V to 5V Input Range
- Advanced CMOS Technology
- DNL: 16-Bits "No Missing Codes"
- 86dB min SINAD with 45kHz Input
- Single +5V Supply Operation
- Utilizes Internal or External Reference
- Serial Output
- Power Dissipation: 132mW Max
- Screening per TM 5004
- QCI per TM5005

SEi 7809LPRP (RP for RAD-PAK ®) high speed 16-bit analog to digital converter features a minimum of 100 kilorad (Si) total dose tolerance. Using SEi radiation hardened RAD-PAK ® packaging technology, the 7809LPRP has the same footprint as ADS7809 and is latchup protected by Space Electronics Latchup Proctection Technology (LPT™). It is a 24 pin, 16-bit sampling analog-to-digital converter using state-of-the-art CMOS structures. The 7809LPRP contains a 16-bit capacitor based SAR A/D with S/H, reference, clock, interface for microprocessor use, and serial output drivers. The 7809LPRP is specified at a 100kHz sampling rate, and guaranteed over the full temperatur range. Laser-trimmed scaling resistors provide various input ranges include ±10V and 0 to 5V, while the innovative design allows operation from a single +5V supply, with power dissipation of under 132mW. Capable of surviving space environments, the 7809LPRP is ideal for satellite, spacecraft, and space probe missions. The patented radiation hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. This product is available in Class S packaging and screening.

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SEi - Radiation Hardened 7809LPRP

16-bit Latchup Protected Analog-to-Digital Converter

7809LPRP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Analog Inputs	$R1_{IN}$ $R2_{IN}$ $R3_{IN}$ CAP REF 1/	-25 -25 -25 V_{ANA}+0.3	+25 +25 +25 AGND2-0.3	V V
Ground Voltage Differences	DGND, AGND2	-0.3	+0.3	V
V_{ANA}			7	V
V_{DIG} to V_{ANA}			+0.3	V
Digital Inputs		-0.3	V_{DIG} +0.3	V
Derated Performance Temperature		-55	+125	°C
Storage Temperature		-65	+150	°C

Note:
1/ Indefinite short to AGND2, momentarily short to V_{ANA}.

7809LPRP DC ACCURACY SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNIT
Integral Linearity Error			+1.5	LSB 1/
Differential Linearity Error			+3, -2	LSB
No Missing Codes	15			Bits
Transition Noise 2/		1.3		LSB
Full Scale Error 3/,4/			±0.5	%
Full Scale Error Drift		±7		ppm/°C
Full Scale Error 3/,4/			±0.5	%
Full Scale Error Drift		±2		ppm/°C
Bipolar Zero Error 3/			±10	mV
Bipolar Zero Error Drift		±2		ppm/°C
Unipolar Zero Error 3/			±3	mV
Unipolar Zero Error Drift		±2		ppm/°C
Recovery to Rated Accuracy after Power Down (1uF Capacitor to CAP)		1		ms
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_D) 4.75V<V_D<5.2V			±8	LSB

Notes:
1/ LSB stands for Least Significant Bit. One LSB is equal to 305uV.
2/ Typical rms noise at worst case transitions and temperatures.
3/ Measured with various fixed resistors.
4/ For bipolar input ranges, full scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also include the effect of offset error.

7809LPRP DIGITAL INPUTS

PARAMETER	MIN	TYP	MAX	UNIT
V_{IL}	-0.3		+0.8	V
V_{IH}	+2.0		V_D+0.3	V
I_{IL}, I_{IH} 1/			±10	uA

Note:
1/ VIL = 0V, VIH = 5V

7809LPRP ANALOG INPUT & THROUGHPUT SPEED

PARAMETER	MIN	TYP	MAX	UNIT
Voltage Ranges	+10V, 0V to 5V			
Impedance	See Table 2.			
Capacitance		35		pF
Conversion Time		7.6	8	µs
Complete Cycle (Aquire and Convert)			10	µs
Throughput Rate	100			kHz

7809LPRP AC ACCURACY SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNIT
Spurious-Free Dynamic Range, f_{IN}=45kHz	90	100		dB1/
Total Harmonic Distortion, f_{IN}=45kHz		-100	-90	dB
Signal-to-(Noise+Distortion), f_{IN}=45kHz -60dB Input	83	88 30		dB
Signal-to-Noise, f_{IN}=45kHz	83	88		dB
Full-Power Bandwidth 2/		250		kHz

Notes:
1/ All specifications in dB are referred to a full-scale ±10V input.
2/ Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB.

7809LPRP SAMPLING DYNAMICS

PARAMETER	MIN	TYP	MAX	UNIT
Aperture Delay		40		ns
Aperture Jitter	Sufficient to meet AC spec			
Transient Response FS Step			2	us
Overvoltage Recovery 1/		150		ns

Notes:
1/ Recovers to specified performance after 2 x FS input overvoltage.

7809LPRP REFERENCE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Internal Reference Voltage	No Load	2.48	2.5	2.52	V
Internal Reference Source Current (Must use ext. buffer)			1		uA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	V
External Reference Current Drain	Ext. 2.5000V Ref			100	uA

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SEi - Radiation Hardened 7809LPRP

16-bit Latchup Protected Analog-to-Digital Converter

7809LPRP DIGITAL OUTPUTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Data Format Data Coding Pipeline Delay	Serial 16-bits Binary Two's Complement or Straight Binary Conversion results only available after completed conversion, Selectable for internal or external data clock.				
Data Clock Internal (Output Only When Transmitting Data) External (Can Run Continually)	 EXT/INT\ LOW EXT/INT\ HIGH	 0.1	 2.3	 10	MHz
V_{OL} V_{OH}	I_{SINK} = 1.6mA I_{SOURCE} = 500uA	 +4		+0.4	V V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5	uA
Output Capacitance	High-Z State			15	pF

7809LPRP POWER SUPPLIES

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	V
V_{ANA}		+4.75	+5	+5.25	V
I_{DIG}			0.3		mA
I_{ANA}			16		mA
Power Dissipation: PWRD LOW PWRD HIGH	V_{ANA} = V_{DIG} = 5V, f_s = 100kHz		 60	132	mW µW

TABLE 1. 7809LPRP CONTROL LINE FUNCTIONS FOR READ AND CONVERT

SPECIFIC FUNCTION	CS	R/C	BUSY	EXT/INT	DATACLK	PWRD	SB/BTC	OPERATION
Initiate Conversion and Output Data Using Internal Clock	1>0	0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n-1" clocked out on DATA synchronized to 16 clock pulses ouput on DATACLK.
	0	1>0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n-1" clocked out on DATA synchronized to 16 clock pulses output on DATACLK.
Initiate Conversion and Output Data Using External Clock	1>0	0	1	1	Input	0	x	Initiates conversion "n".
	0	1>0	1	1	Input	0	x	Initiates conversion "n".
	1>0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion "n" clocked out synchronized to external DATACLK.
	1>0	1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n-1" clocked out synchronized to external DATACLK.[1] Conversion "n" in process.
	0	0>1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n-1" clocked out synchronized to external DATACLK.[1] Conversion "n" in process.
Incorrect Conversions	0	0	0>1	x	x	0	x	CS or R/C must be HIGH or a new conversion will be initiated without time for acquisition.
Power Down	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed.
	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.
Selecting Output Format	x	x	x	x	x	x	0	Serial data is output in Binary Two's Complement format.
	x	x	x	x	x	x	1	Serial data is output in Straight Binary format.

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Table 2. 7809LPRP Input Range Connection

Analog Input Range	Connect $R1_{IN}$ via 200Ω to	Connect $R2_{IN}$ via 100Ω to	Connect $R3_{IN}$ to	Impedance
+10V	VIN	AGND	CAP	22.9 kΩ
+5V	AGND	VIN	CAP	13.3 kΩ
+3.3V	VIN	VIN	CAP	10.7 kΩ
0V to 10V	AGND	VIN	AGND	13.3 kΩ
0V to 5V	AGND	AGND	VIN	10.0 kΩ
0V to 4V	VIN	AGND	VIN	10.7kΩ

Table 3. 7809LPRP Conversion and Data Timing
T_A = -40°C to +85°C.

Symbol	Description	Min	Typ	Max	Unit
t1	Convert Pulse Width	40		6000	ns
t2	BUSY Delay			65	ns
t3	BUSY LOW			8	
t4	BUSY Delay after End of Conversion		220		ns
t5	Aperture Delay		40		ns
t6	Conversion Time		7.6	8	µs
t7	Acquisition Time			2	µs
t6+t7	Throughput Time		9	10	µs
t8	R/C Low to DATACKL Delay		450		ns
t9	DATACLK Period		440		ns
t10	Data Valid to DATACLK HIGH Delay	20	75		ns
t11	Data Valid afer DATRACLK LOW Delay	100	125		ns
t12	External DATACLK	100			ns
t13	External DATACLK HIGH	20			ns
t14	External DATACLK LOW	30			ns
t15	DATACLK HIGH Setup Time	20		t12+5	ns
t16	R/C to CS Setup Time	10			ns
t17	SYNC Delay After DATACLK High	15		35	ns
t18	Data Valid Delay	25		55	ns
t19	CS to Rising Edge Delay	25			ns
t20	Data Available after CS LOW	0			µs

Table 4. 7809LPRP CONVERSION DATA TIMING

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY TWO'S COMPLEMENT (SB/BTC LOW)		STRAIGHT BINARY (SB/BTC HIGH)	
							BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
Full-Scale Range	±10	±5	±3.33V	0V to 10V	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	305µV	153µV	102µV	153µV	76µV	61µV				
+Full Scale (FS – 1LSB)	9.999695V	4.999847V	3.333231V	9.999847V	4.999924V	3.999939V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0V	0V	0V	5V	2.5V	2V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB Below Midscale	–305µV	–153µV	–102µV	4.999847V	2.499924V	1.999939V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
–Full Scale	–10V	–5V	–3.333333V	0V	0V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

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Figure I. 7809LPRP CONVERSION TIMING

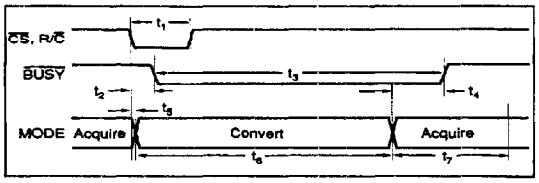

Figure II. 7809LPRP Serial Data Timing Using Internal Clock ($\overline{CS}$, EXT/$\overline{INT}$ and TAG tied LOW)

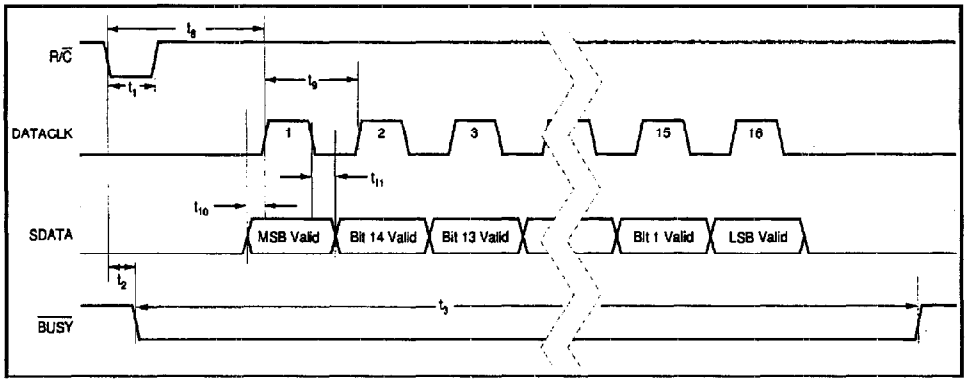

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Figure IIIA. 7809LPRP Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ tied HIGH). Read After Conversion

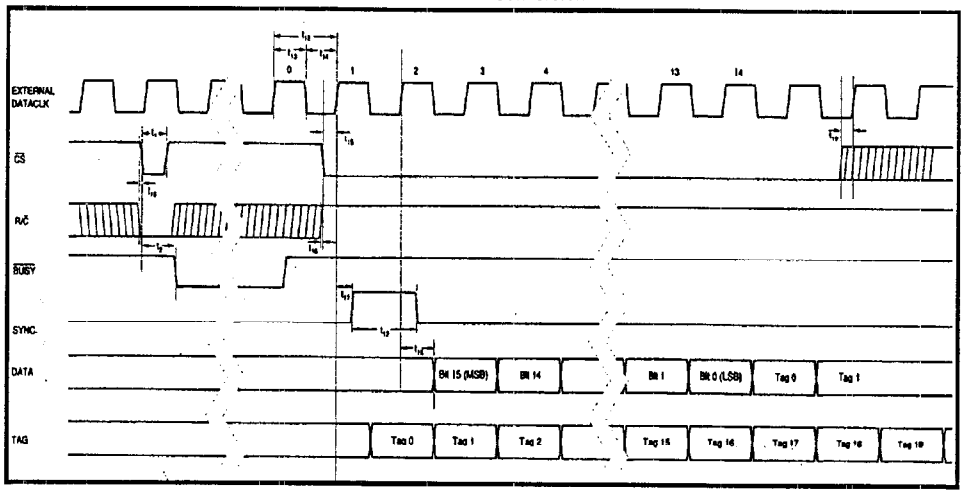
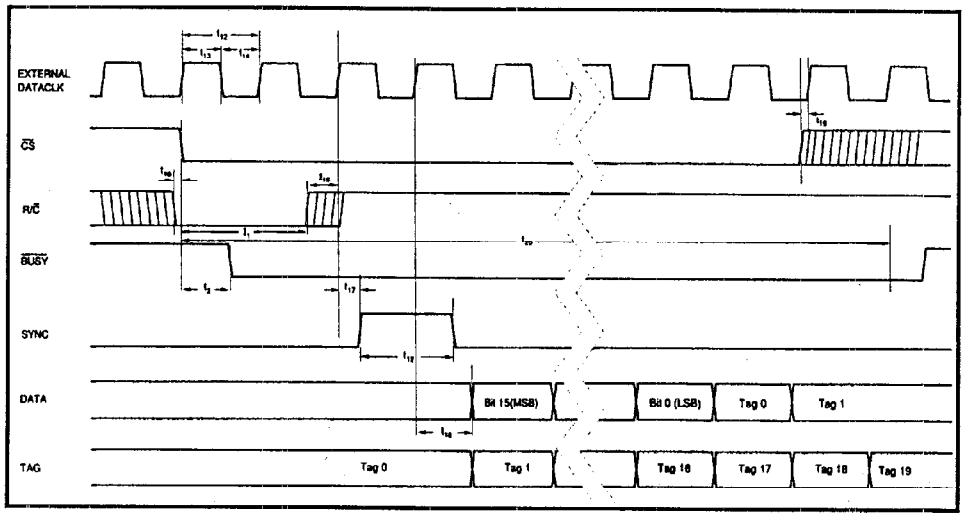


Figure IIIB. 7809LPRP Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ tied HIGH). Read During Conversion



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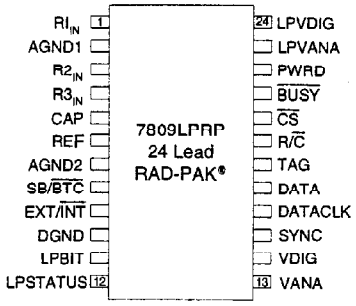
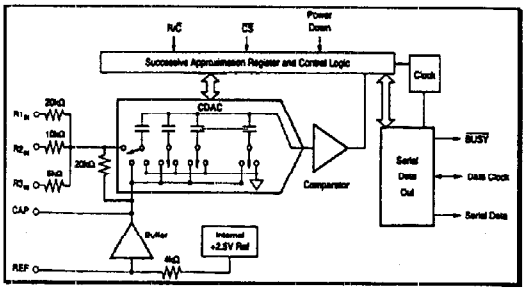
SEi - Radiation Hardened **7809LPRP**

16-bit Latchup Protected Analog-to-Digital Converter





Features:

- 16-Bit Organization
- RAD-PAK® Technology Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- Latch-up Protection Technology (LPT™)
- Same Footprint as ADS7809
- Package: 24 Pin RAD-PAK® Flat Package
- 100 kHz min Sampling Rate
- ±10V and 0V to 5V Input Range
- Advanced CMOS Technology
- DNL: 16-Bits "No Missing Codes"
- 86dB min SINAD with 45kHz Input
- Single +5V Supply Operation
- Utilizes Internal or External Reference
- Serial Output
- Power Dissipation: 132mW Max
- Screening per TM 5004
- QCI per TM5005

SEi 7809LPRP (RP for RAD-PAK ®) high speed 16-bit analog to digital converter features a minimum of 100 kilorad (Si) total dose tolerance. Using SEi radiation hardened RAD-PAK ® packaging technology, the 7809LPRP has the same footprint as ADS7809 and is latchup protected by Space Electronics Latchup Proctection Technology (LPT™). It is a 24 pin, 16-bit sampling analog-to-digital converter using state-of-the-art CMOS structures. The 7809LPRP contains a 16-bit capacitor based SAR A/D with S/H, reference, clock, interface for microprocessor use, and serial output drivers. The 7809LPRP is specified at a 100kHz sampling rate, and guaranteed over the full temperatur range. Laser-trimmed scaling resistors provide various input ranges include ±10V and 0 to 5V, while the innovative design allows operation from a single +5V supply, with power dissipation of under 132mW. Capable of surviving space environments, the 7809LPRP is ideal for satellite, spacecraft, and space probe missions. The patented radiation hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. This product is available in Class S packaging and screening.

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SEi - Radiation Hardened 7809LPRP

16-bit Latchup Protected Analog-to-Digital Converter

7809LPRP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Analog Inputs	$R1_{IN}$ $R2_{IN}$ $R3_{IN}$ CAP REF 1/	-25 -25 -25 V_{ANA}+0.3	+25 +25 +25 AGND2-0.3	V V
Ground Voltage Differences	DGND, AGND2	-0.3	+0.3	V
V_{ANA}			7	V
V_{DIG} to V_{ANA}			+0.3	V
Digital Inputs		-0.3	V_{DIG} +0.3	V
Derated Performance Temperature		-55	+125	°C
Storage Temperature		-65	+150	°C

Note:
1/ Indefinite short to AGND2, momentarily short to V_{ANA}.

7809LPRP DIGITAL INPUTS

PARAMETER	MIN	TYP	MAX	UNIT
V_{IL}	-0.3		+0.8	V
V_{IH}	+2.0		V_D+0.3	V
I_{IL}, I_{IH} 1/			±10	uA

Note:
1/ VIL = 0V, VIH = 5V

7809LPRP ANALOG INPUT & THROUGHPUT SPEED

PARAMETER	MIN	TYP	MAX	UNIT
Voltage Ranges	+10V, 0V to 5V			
Impedance	See Table 2.			
Capacitance		35		pF
Conversion Time		7.6	8	µs
Complete Cycle (Aquire and Convert)			10	µs
Throughput Rate	100			kHz

7809LPRP DC ACCURACY SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNIT
Integral Linearity Error			±1.5	LSB 1/
Differential Linearity Error			+3, -2	LSB
No Missing Codes	15			Bits
Transition Noise 2/		1.3		LSB
Full Scale Error 3/,4/			±0.5	%
Full Scale Error Drift		±7		ppm/°C
Full Scale Error 3/,4/			±0.5	%
Full Scale Error Drift		±2		ppm/°C
Bipolar Zero Error 3/			±10	mV
Bipolar Zero Error Drift		±2		ppm/°C
Unipolar Zero Error 3/			±3	mV
Unipolar Zero Error Drift		±2		ppm/°C
Recovery to Rated Accuracy after Power Down (1uF Capacitor to CAP)		1		ms
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_D) 4.75V<V_D<5.2V			±8	LSB

Notes:
1/ LSB stands for Least Significant Bit. One LSB is equal to 305uV.
2/ Typical rms noise at worst case transitions and temperatures.
3/ Measured with various fixed resistors.
4/ For bipolar input ranges, full scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also include the effect of offset error.

7809LPRP AC ACCURACY SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNIT
Spurious-Free Dynamic Range, f_{IN}=45kHz	90	100		dB1/
Total Harmonic Distortion, f_{IN}=45kHz		-100	-90	dB
Signal-to-(Noise+Distortion), f_{IN}=45kHz -60dB Input	83	88 30		dB
Signal-to-Noise, f_{IN}=45kHz	83	88		dB
Full-Power Bandwidth 2/		250		kHz

Notes:
1/ All specifications in dB are referred to a full-scale ±10V input.
2/ Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB.

7809LPRP SAMPLING DYNAMICS

PARAMETER	MIN	TYP	MAX	UNIT
Aperture Delay		40		ns
Aperture Jitter	Sufficient to meet AC spec			
Transient Response FS Step			2	us
Overvoltage Recovery 1/		150		ns

Notes:
1/ Recovers to specified performance after 2 x FS input overvoltage.

7809LPRP REFERENCE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Internal Reference Voltage	No Load	2.48	2.5	2.52	V
Internal Reference Source Current (Must use ext. buffer)			1		uA
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	V
External Reference Current Drain	Ext. 2.5000V Ref			100	uA

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SEi - Radiation Hardened 7809LPRP

16-bit Latchup Protected Analog-to-Digital Converter

7809LPRP DIGITAL OUTPUTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Data Format Data Coding Pipeline Delay	Serial 16-bits Binary Two's Complement or Straight Binary Conversion results only available after completed conversion, Selectable for internal or external data clock.				
Data Clock Internal (Output Only When Transmitting Data) External (Can Run Continually)	 EXT/INT\ LOW EXT/INT\ HIGH	 0.1	 2.3	 10	MHz
V_{OL} V_{OH}	I_{SINK} = 1.6mA I_{SOURCE} = 500uA	 +4		+0.4	V V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5	uA
Output Capacitance	High-Z State			15	pF

7809LPRP POWER SUPPLIES

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	V
V_{ANA}		+4.75	+5	+5.25	V
I_{DIG}			0.3		mA
I_{ANA}			16		mA
Power Dissipation: PWRD LOW PWRD HIGH	V_{ANA} = V_{DIG} = 5V, f_s = 100kHz		 60	132	mW µW

TABLE 1. 7809LPRP CONTROL LINE FUNCTIONS FOR READ AND CONVERT

SPECIFIC FUNCTION	$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	EXT/$\overline{INT}$	DATACLK	PWRD	SB/$\overline{BTC}$	OPERATION
Initiate Conversion and Output Data Using Internal Clock	1>0	0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n−1" clocked out on DATA synchronized to 16 clock pulses ouput on DATACLK.
	0	1>0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n−1" clocked out on DATA synchronized to 16 clock pulses output on DATACLK.
Initiate Conversion and Output Data Using External Clock	1>0	0	1	1	Input	0	x	Initiates conversion "n".
	0	1>0	1	1	Input	0	x	Initiates conversion "n".
	1>0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion "n" clocked out synchronized to external DATACLK.
	1>0	1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n−1" clocked out synchronized to external DATACLK.[1] Conversion "n" in process.
	0	0>1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n−1" clocked out synchronized to external DATACLK.[1] Conversion "n" in process.
Incorrect Conversions	0	0	0>1	x	x	0	x	$\overline{CS}$ or R/$\overline{C}$ must be HIGH or a new conversion will be initiated without time for acquisition.
Power Down	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed.
	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.
Selecting Output Format	x	x	x	x	x	x	0	Serial data is output in Binary Two's Complement format.
	x	x	x	x	x	x	1	Serial data is output in Straight Binary format.

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Table 2. 7809LPRP Input Range Connection

Analog Input Range	Connect $R1_{IN}$ via 200Ω to	Connect $R2_{IN}$ via 100Ω to	Connect $R3_{IN}$ to	Impedance
+10V	VIN	AGND	CAP	22.9 kΩ
+5V	AGND	VIN	CAP	13.3 kΩ
+3.3V	VIN	VIN	CAP	10.7 kΩ
0V to 10V	AGND	VIN	AGND	13.3 kΩ
0V to 5V	AGND	AGND	VIN	10.0 kΩ
0V to 4V	VIN	AGND	VIN	10.7kΩ

Table 3. 7809LPRP Conversion and Data Timing
T_A = -40°C to +85°C.

Symbol	Description	Min	Typ	Max	Unit
t1	Convert Pulse Width	40		6000	ns
t2	BUSY Delay			65	ns
t3	BUSY LOW			8	
t4	BUSY Delay after End of Conversion		220		ns
t5	Aperture Delay		40		ns
t6	Conversion Time		7.6	8	µs
t7	Acquisition Time			2	µs
t6+t7	Throughput Time		9	10	µs
t8	R/C Low to DATACKL Delay		450		ns
t9	DATACLK Period		440		ns
t10	Data Valid to DATACLK HIGH Delay	20	75		ns
t11	Data Valid afer DATRACLK LOW Delay	100	125		ns
t12	External DATACLK	100			ns
t13	External DATACLK HIGH	20			ns
t14	External DATACLK LOW	30			ns
t15	DATACLK HIGH Setup Time	20		t12+5	ns
t16	R/C to CS Setup Time	10			ns
t17	SYNC Delay After DATACLK High	15		35	ns
t18	Data Valid Delay	25		55	ns
t19	CS to Rising Edge Delay	25			ns
t20	Data Available after CS LOW	6			µs

Table 4. 7809LPRP CONVERSION DATA TIMING

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY TWO'S COMPLEMENT (SB/BTC LOW)		STRAIGHT BINARY (SB/BTC HIGH)	
							BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
Full-Scale Range	±10	±5	±3.33V	0V to 10V	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	306µV	153µV	102µV	153µV	76µV	61µV				
+Full Scale (FS – 1LSB)	9.999695V	4.999847V	3.333231V	9.999847V	4.999924V	3.999939V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0V	0V	0V	5V	2.5V	2V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB Below Midscale	–305µV	–153µV	–102µV	4.999847V	2.499924V	1.999939V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
–Full Scale	–10V	–5V	–3.333333V	0V	0V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

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Figure I. 7809LPRP CONVERSION TIMING

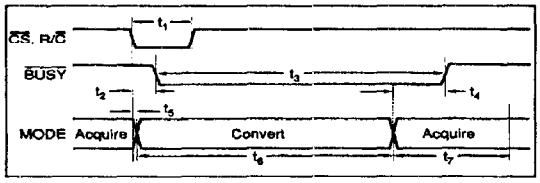

Figure II. 7809LPRP Serial Data Timing Using Internal Clock ($\overline{CS}$, EXT/$\overline{INT}$ and TAG tied LOW)

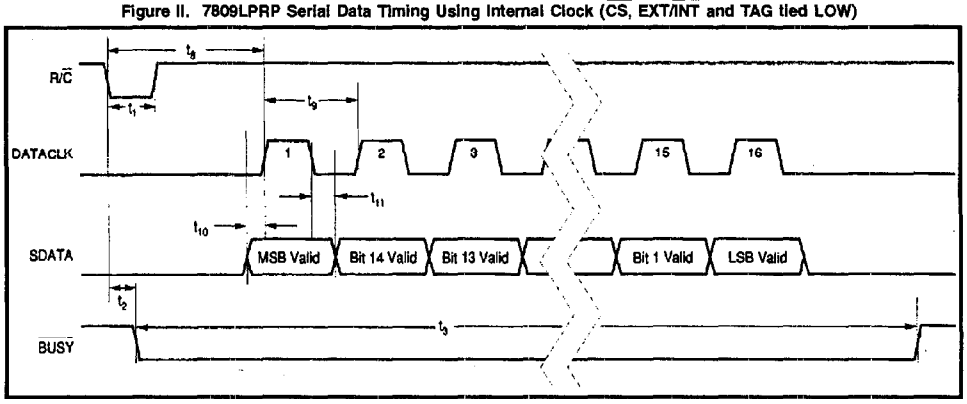

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Figure IIIA. 7809LPRP Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ tied HIGH). Read After Conversion

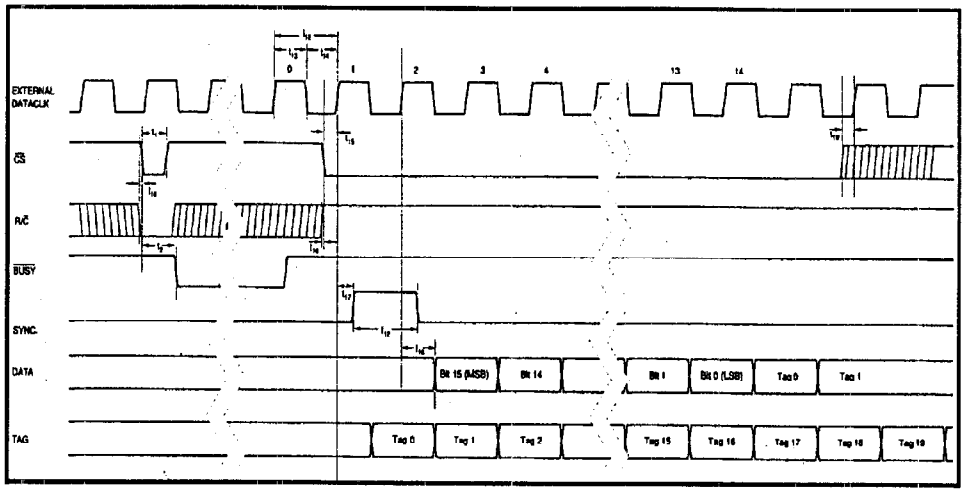

Figure IIIB. 7809LPRP Conversion and Read Timing with External Clock (EXT/$\overline{INT}$ tied HIGH). Read During Conversion

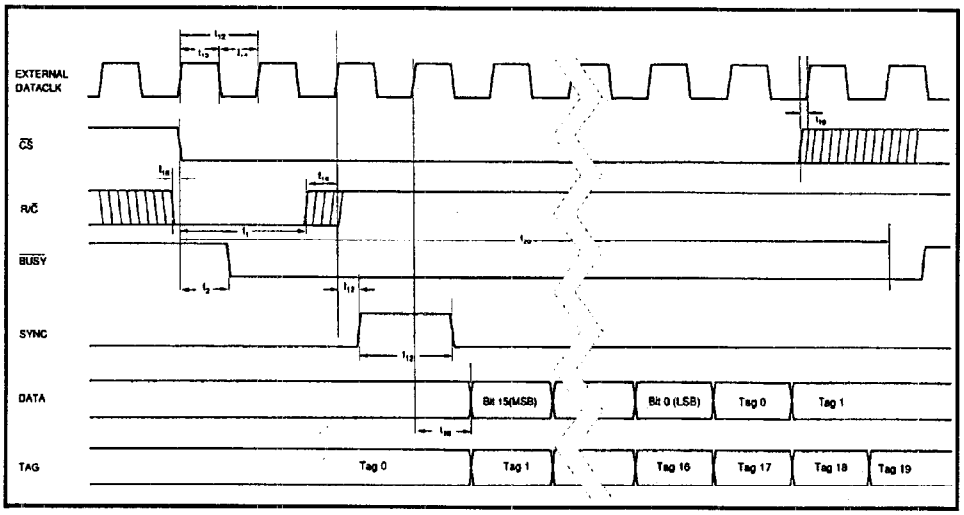

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Figure IVA. 7809LPRP Offset/Gain Circuits for Unipolar Input Ranges

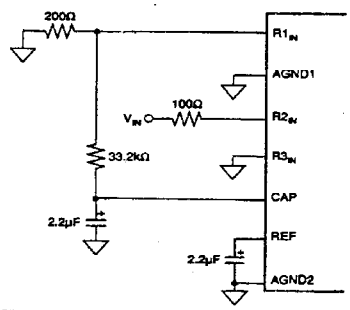
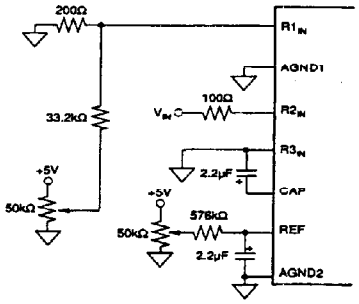
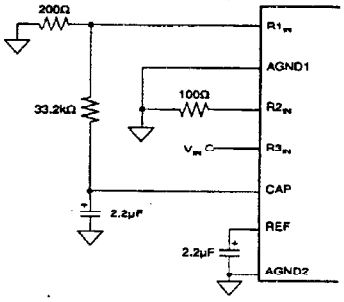
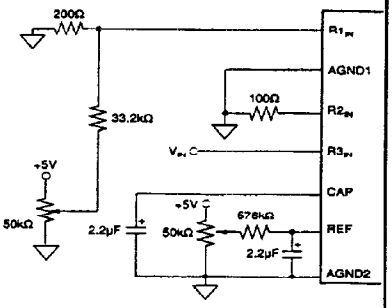
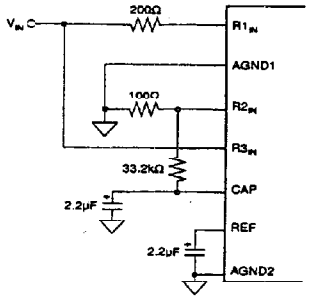
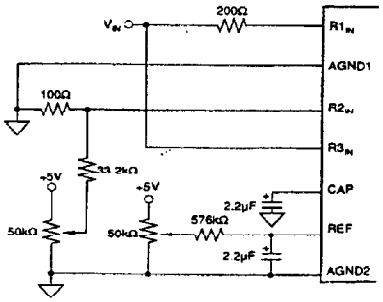
Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
0V – 10V		
0V – 5V		
0V – 4V		

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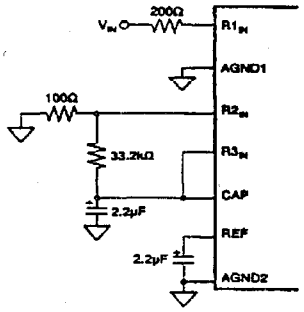
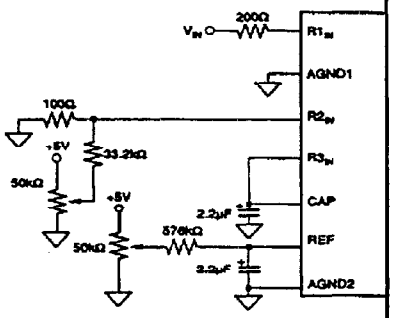
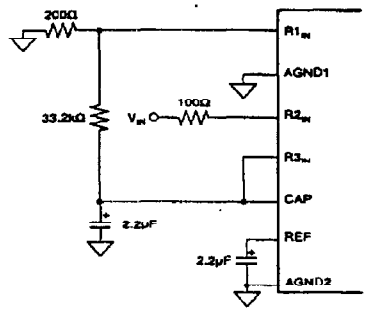
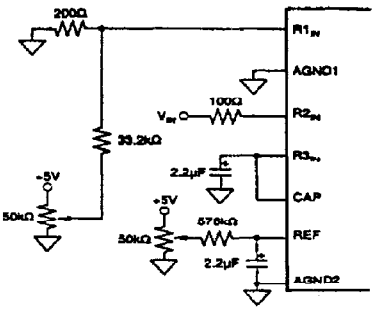
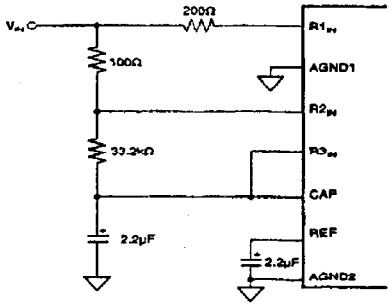
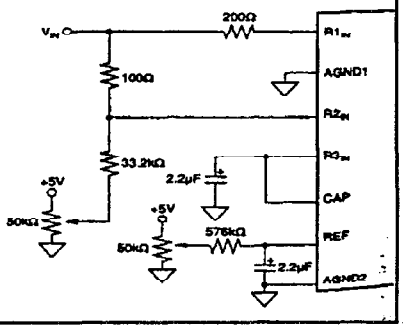
Figure IVB. 7809LPRP Offset/Gain Circuits for Bipolar Input Ranges

Input Range	Without Trim	With Trim (Adjust offset first at 0V, then adjust gain)
±10V		
±5V		
±3.33V		

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SEi - Radiation Hardened **7809LPRP**

16-bit Latchup Protected Analog-to-Digital Converter

7809LPRP PINOUT DESCRIPTION

PIN#	NAME	DESCRIPTION
1	R1IN	Analog Input.
2	AGND1	Analog Ground. Used internally as ground reference point.
3	R2IN	Analog Input.
4	R3IN	Analog Input.
5	CAP	Reference Buffer Capacitor. 2.2uF Tantalum to ground.
6	REF	Reference Input/Output. 2.2uF tantalum capacitor to ground.
7	AGND2	Analog Ground.
8	SB/$\overline{BTC}$	Select Straight Binary or Binary Twos Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Twos Complement format.
9	EXT/$\overline{INT}$	Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 16 clock pulses output on DATACLK.
10	DGND	Digital Ground.
11	LPBIT	Built In Test function of the latchup protection. Drive LOW during normal operation.
12	LPSTATUS	Latchup Protection Status Output. LPSTATUS when HIGH indicates latchup protection is active and output data is invalid.
13	VANA	Analog Supply Input. Nominally +5V.
14	VDIG	Digital Supply Input. Nominally +5V.
15	SYNC	Synch Output. If EXT/INT is HIGH, either a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW or a falling edge on CS with R/C HIGH will output a pulse on SYNC synchronized to the external DATACLK.
16	DATACLK	Either an input or an output depending on the EXT/$\overline{INT}$ level. Output data will be synchronized to this clock mode. If EXT/$\overline{INT}$ is LOW, DATACLK will transmit 16 pulses after each conversion, and then remain LOW between conversions.
17	DATA	Serial Data Ouput. Data will be synchronized to DATACLK, with the format determined by the level of SB/BTC. In the external clock mode, after 16-bits of data, the 7809LPRP will output the level input on TAG as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH. If EXT/$\overline{INT}$ is LOW, data will be valid on both the rising and falling edges of DATACLK, and betweem conversions DATA will stay at the level of the TAG input when the conversion was started.
18	TAG	Tag Input for use in external clock mode. If EXT/$\overline{INT}$ is HIGH, the digital data input on TAG will be output on DATA with a delay of 16 DATACLK pulses as long as $\overline{CS}$ is LOW and R/$\overline{C}$ is HIGH.
19	R/$\overline{C}$	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. When EXT/$\overline{INT}$ is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/$\overline{INT}$ is HIGH, a rising edge on R/$\overline{C}$ with $\overline{CS}$ LOW, or a falling edge on $\overline{CS}$ with R/$\overline{C}$ HIGH, transmits a pulse on SYNC and initiates the transmission of daAta from the previous conversion.
20	$\overline{CS}$	Chip Select. Internally ORed with R/$\overline{C}$.
21	BUSY	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. $\overline{CS}$ or R/$\overline{C}$ must be HIGH when BUSY rises, or another conversion will start without time for signal acquisition.
22	PWRD	Power Down Input. If HIGH, conversions are inhibited and poewr consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
23	LPVANA	Latchup Protection Analog Supply.
24	LPVDIG	Latchup Protection Digital Supply.

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LPT™Operation

Latchup Protection Technology (LPT™) automatically detects an increase in the supply current of the 7809ALPRP converter due to a single event effect and internally cycles the power to the converter off, then on, which restores the steady state operation of the device. A simplified block diagram of the 7809ALPRP circuitry is shown in Figure V. The circuitry consists of a protected device, the ADS7809 die, a current sensor, a power switch, and a status output driver.

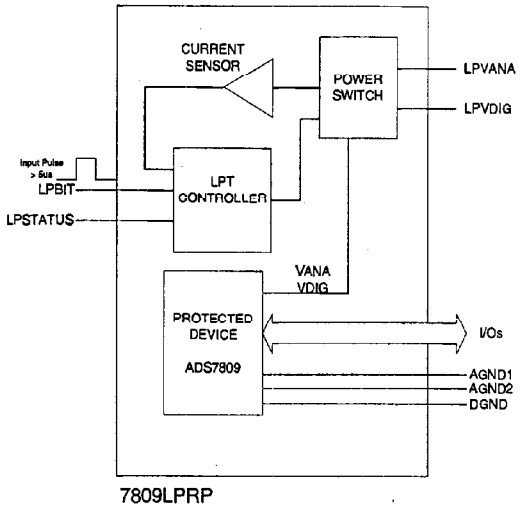

Figure V. Latchup Protection Technology Block Diagram

Differences Between the 7809LPRP and the ADS7809

Because the 7809LPRP uses the ADS7809 die to perform the analog to digital conversion function its operation and performance is very similar to the ADS7809 packaged part from Burr-Brown. In general the operation and application will be the same for both parts. There are two primary differences: the Built In Test (LPBIT) operation of the Latchup Protection circuitry and the operation of the LPT™ LPSTATUS pins.

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SEi - Radiation Hardened **7809LPRP**

16-bit Latchup Protected Analog-to-Digital Converter

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The 7809LPRP LPBIT pin serves a Built In Test function. An active high TTL pulse of sufficient duration (~5µs) applied to the LPBIT input will trigger the latchup protection function. This input shall be low during normal operation. If Built In Test is not used, this input should be grounded.

The additional supply inputs LPVANA and LPVDIG power both the analog and digital circuitry through the LPT™ current sensor and power switch.

The primary functional difference between the ADS7809 and the 7809LPRP is the addtional pin LPSTATUS. A low level LPSTATUS signal indicates that a single event induced latchup current was detected by the LPT™ circuitry causing power to be removed from the protected device. **CAUTION: During the time that power is removed from the protected device, it is critical that external circuitry driving the device I/O pins does not backdrive the device supply. Backdriving the supply could contribute to an extended or even a permanent latchup condition.**

In order to prevent backdriving the supply, the LPSTATUS signal should be used in the system to tri-state or gate external I/O drive circuits to a low state. Similarly, if the data outputs are connected to a bus with other bus driver circuits, all external data bus drivers must be tri-stated and individual pull up resistors to the supply voltage (if used on the data bus) must not be less than 10 KOhms typical to assure proper single event effect recovery. Tri-stating of inputs should occur within 100 nsec after the rise of the status pin.

LPSTATUS can also be used to generate an input to the system data processor indicating that an LPT™ cycle has occurred and the protected device output accuracy may not be met until after the respective recovery time to the event. The LPSTATUS signal is generated from an advanced CMOS logic gate output. This output may not exhibit a monotonic fall time and may even oscillate briefly while power is being restored to the protected device and the decoupling capacitance is charged. Loading on the LPSTATUS output should be minimized because this signal is used internally by the 7809LPRP. It is recommended that load current not exceed 2 mA and load capacitance be kept well below 1000 pF.

A summary of the additional pin differences between the ADS7809 and 7809LPRP is provided in Table 1.

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PIN #	ADS7809	7809LPRP	PIN DIFFERENCE DESCRIPTION
1-10	Various	Various	Equivalent function to ADS7809 pins 1-10 respectively. Timing specifications change slightly (0-10ns) for the 7809LPRP due to the latchup protection circuitry on ADS7809 die inputs.
15-22	Various	Various	Equivalent function to ADS7809 pins 11-18 respectively. Timing specifications change slightly (0-10ns) for the 7809LPRP due to the latchup protection circuitry on ADS7809 die inputs.
11	---	LPBIT	A Built In Test function of latchup protection. A TTL high level pulse for > 5 microseconds duration on this input will trigger latchup protection of the device. This input shall be low when normal operation.
12	---	LPSTATUS	Latchup protection status output. This TTL level output is low during normal operation and goes high within 1us of the power being removed from the latchup protected device. When latchup protection is triggered, this output will go high for the duration of the time that power is removed from the protected device (50us). All outputs except LPSTATUS are invalid during the time that power is removed from the ADS7809 die. This output goes low within 1us of the power being re-applied tot he protected device. Functional operation of the device is within 25 us after the LPSTATUS output returns low with degraded accuracy due to the latchup protection power transient to the ADS7809 die. Full accuracy is restored 500ms later. This output can be used to inform the system processor of the latchup protection trigger and the subsequent degraded accuracy in the 7809LPRP output data. I/O pins must not be driven high while this signal is active.
23	---	LPVANA	Latchup protected analog supply pin to the ADS7809 die. Decouple to analog ground with 0.1uF ceramic capacitor. Do not exceed 0.2uF. Do not connect to VDIG and VANA.
24	---	LPVDIG	Latchup protected digital supply pin to the ADS7809 die. Decouple to digital ground with 0.1uF ceramic capacitor. Do not exceed 0.2uF. Do not connect to VDIG and VANA.

Table 1. ADS7809 and 7809LPRP Pin Differences

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Single Event Latchup Protection Of Integrated Circuits

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Abstract.

This paper will report the test results from the development of the single event latchup protection circuitry (referred to as Space Electronics Inc.'s (SEI's) LPT™ technology) for several integrated circuits which are known to latchup at unacceptably low LET energies for space applications. Two devices were evaluated with LPT™; the ADS7805 16 bit analog to digital converter and the GF10009 FPGA (Gatefield's 9000 gate flash programmable gate array).

I. INTRODUCTION

Many commercially available advanced technology CMOS and bipolar integrated circuits are latchup susceptible to single event effects caused by heavy ions or protons from cosmic rays or solar flares making them unsuitable for satellite applications. Remanufacturing the integrated circuits on an inherently SEL immune process has been an expensive and technically difficult option as is the alternate option of incorporating latchup protection and recovery circuitry in the spacecraft system electronics.

Space Electronics Inc. has developed several different circuits which provide protection and recovery of integrated circuits known to exhibit single event induced latchup. These circuits are integrated within the same package as the susceptible integrated circuit using MCM and modern packaging technology resulting in a device level solution providing minimum cost and minimum impact on the system.

The LPT™ circuit was designed to provide the following features to protect and recover the susceptible integrated circuit device:

a. Provide current limiting to the device.
b. Detect the increase in current during the SEL event above a preset threshold.
c. Force a shutdown of the protected device when the threshold is exceeded.
d. Hold the device in the shut down mode for a preset time interval.
e. Return the device supply voltage to its original operating level.

The LPT™ circuitry (patent pending) has the potential to be applied to a wide variety of susceptible devices. The specific implementation details such as current latchup protection threshold and supply off time are determined by characterization of the susceptible devices at a heavy ion facility. The LPT™ device impacts a satellite component system by converting a Single Event Latchup (SEL) into a recoverable event. Using mission specific or orbit radiation data, recoverable event rates can be calculated. The rate and number of these recoverable events is dependent on the fluence, energy, and species of radiation encountered by the device during the particular mission [1].

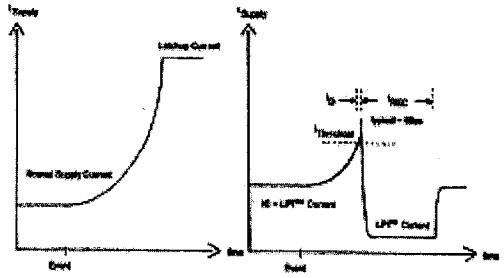
II. LPT™ CIRCUIT

The first device selected for latchup protection was the ADS7805. The preliminary circuit design and analysis was based on protecting the ADS7805 device, which is susceptible to SEL at low Linear Energy Transfer (LET) levels.

The ADS7805 integrated circuit draws current from an analog and digital supply pin. The LPT™ circuit must sense the current into the supply pins and when the latchup current threshold is exceeded, remove the supply voltage from the latched device. During the time that the supply voltage is removed from the device, the supply current draw will come exclusively from the LPT™ circuit. After a set time interval required for the latchup to clear, the LPT™ circuit reapplies the supply voltage to the device and normal operation is restored.

Figure 1 shows the supply current with and without a protection circuit during a single event latchup. The LPT™ circuit will have a latchup current threshold, $I_{Threshold}$, an activation delay time, t_D, and recovery time, t_{REC}, as shown in figure 1 (b). The LPT™ circuit is activated when the supply current exceeds the $I_{Threshold}$ value, the supply current is turned off (grounded) within time t_D after $I_{Threshold}$ is reached. The device is off for time period t_{REC}. This can be compared with

the unprotected latchup supply current response shown in figure 1(a) where the normal operating current rises to the latchup current in response to a single event latchup.



(a) unprotected (b) protected circuit

Figure 1 Supply current waveforms

Two types of circuits were designed to protect and recover the ADS7805 from SEL. The primary components of the first circuit were a dual comparator and a logic level P channel MOSFET. One comparator was used to detect when the latchup current threshold was exceeded and provide a limited duration control pulse when this occurred. The second comparator provided a status output to indicate to the system that latchup had been detected and power was removed from the ADS7805. The logic level P channel MOSFET was used as a high side power switch to the ADS7805.

The second circuit used a specialized integrated circuit, the LTC1153 Auto Reset Electronic Circuit Breaker, available from Linear Technologies, Inc. [2] along with an N channel MOSFET. The LTC1153 provided latchup threshold detection, gate drive to the MOSFET including timed shutoff and status output to the system. The N-Channel MOSFET was operated as a high side power switch to the ADS7805.

In both LPT™ circuits, the analog and digital supply inputs to the device were tied together through a low value current sense resistor and powered by a single supply input.

III. VALIDATION TEST RESULTS

Both LPT™ circuit types were tested at the JPL Californium-252 source. Additionally, two different comparators devices were tested in the comparator circuit. One comparator exhibited higher speed with higher power, while the second comparator exhibited lower speed and significantly lower power.

The test circuit consisted of a breadboard of each LPT™ circuit type, a de-lidded ADS7805 (the target of the radiation), and a 16 bit digital to analog converter circuit which provided a composite monitor of the ADS7805 parallel data output. The status signal was used to trigger a digital storage scope set to capture the supply current response and the composite monitor response. A full scale sinusoidal input signal was provided to the ADS7805 during all testing, and the composite output was continuously monitored by a DMM for loss of functional operation.

The test results from the JPL Californium-252 test are shown in table 1. The fragments from the Californium source exhibit an LET of ~42 MeV-cm^2/mg. Latchup protection and recovery was demonstrated for both circuit types over a range of input conditions, LPT™ delay and recovery times.

Note that under one test condition latchup recovery did not occur. This was due to the applied voltages and related current limiting on the digital input pins to the ADS7805. The first condition occurred with the CS, R/C, and BYTE signals tied to +5V (chip not selected) each through a 91 Ohm series resistor. When the resistors were increased to 511 Ohms, latchup recovery occurred. Values between 91 and 511 Ohms were not tested. This result showed that not only does the supply voltage have to be removed, but the inputs must be carefully considered to assure that backdriving the supply through input pins does not sustain the latchup.

Subsequent testing of the LPT™ circuitry was performed at Texas A&M University cyclotron. The primary concern of this testing was to determine if there were any latchup modes that were not exhibited with the limited LET characterization available from the Californium-252 source. Since the main concern of this test was the SEL response of the ADS7805, only the LTC1153 based circuit was tested. The results of this testing are summarized in table 2. The LPT™ circuit successfully recovered the ADS7805 from all SELs over an LET range of 14 - 80 MeV-cm^2/mg. Additionally, this testing bounded the SEL threshold of the ADS7805 between 9.9 and 14 MeV-cm^2/mg.

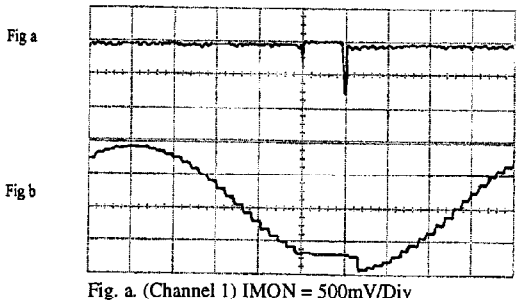


Fig. a. (Channel 1) IMON = 500mV/Div
Fig. b. (Channel 2), VOUT; 5 V/Div

Figure 2. 7805LRP Response to a Single Event Latchup, 50µs recovery

Figure 2 shows the LPT™ operation in response to a single event latchup. Curve (a) shows the latchup current occurring (spike at center of trace). The current is then cycled off then on. The spike one division later corresponds to the recharging of the decoupling capacitors attached to the ADS7805 supply pins. Figure 2b shows the effect of the LPT protection and recovery on the ADS7805 output. Functional recovery occurs approximately 70 µs after latchup, although the scale factor takes additional time to recover full accuracy. All Y axis are 50 µs/Div.

No destructive functional failures of any of the ADS7805 devices tested occurred during either radiation or flash testing.

Table 1: LPT™ Test Results at JPL Californium-252 Source

LPT Circuit	Operation	Series Rs (Ohm)	tD (µs)	Latchup Current (mA)	Recovery	T_{REC} (ms)	LET (Mev-cm²/mg)
LTC1153	Normal	132	19	159-133	Yes	2.5	42
Slow Comparator	Normal	113	15	159-133	Yes	2.5	42
Slow Comparator	All Inputs High	91	15	159-133	No		42
Slow Comparator	All Inputs High	1000	15	159-133	Yes	2.5	42
Fast Comparator	All Inputs High	511	1.5	159-133	Yes	2.5	42
Fast Comparator	Normal	511	1.5	159-133	Yes	2.5	42
Fast Comparator	Normal	511	1.5	159-133	Yes	45 µs	42

Table 2: LPT™ Test Results at Texas A&M University Cyclotron

LPT Circuit	Operation	Series Rs (Ohm)	tD (µs)	Latchup Current (mA)	Recovery	T_{REC} (ms)	LET Mev-cm²/mg
LTC1153	Normal	1k	19	None	n/a	2.5	7
LTC1153	Normal	1k	19	None	n/a	2.5	9.9
LTC1153	Normal	1k	19	267	Yes	2.5	14
LTC1153	Normal	1k	19	146 - 267	Yes	2.5	40
LTC1153	Normal	1k	19	146 - 267	Yes	2.5	56.6
LTC1153	Normal	1k	19	146 - 267	Yes	2.5	80

IV. IMPLEMENTATION

Since the operating and latchup currents vary for different devices each device needs to be characterized for these parameters before an LPT™ can be designed for that particular device. The characterization of two such devices are described below.

A. ADS7805 Testing

Test results, as reported in JPL's radiation effects database [3] from a Brookhaven National Laboratory (BNL) heavy ion test conducted on 12/6/94, bounded SEL threshold for the ADS7805 below 38 MeV-cm²/mg. This threshold level created a high probability of latchup in a space environment, making this device unsuitable for space applications. The latchup current level from the BNL test was not reported. Typical operating current of the ADS7805 is specified as 16.3 mA for both the analog and digital 5V supply. The maximum specified operating current [4] for the device is 20 mA.

An interesting characteristic of the ADS7805 die was that latchup could be induced with a high intensity light source. We were able to trigger latchup by exposing de-lidded devices to the flash from a 35mm camera flash bulb. Typical peak photoelectric currents were measured on the supply inputs at ~650 mA with a duration of 2 ms. After the flash

induced current dissipated, the device latchup current was measured to be 110 mA. This latchup characteristic of the ADS7805 was used to electrically test and debug the LPT™ circuits during development and prior to radiation exposure.

Heavy ion characterization and validation of the ADS7805 with the LPT™ circuitry was performed using the Jet Propulsion Laboratories (JPL) Californium -252 source at Pasadena CA and also using the Texas A&M University Cyclotron facility. Latchup protection and recovery of the ADS7805 was demonstrated at both of these facilities. Peak latchup current was measured between 146 and 267 mA and device recovery was shown with supply off times of 45 µsec and 2.5 msec. Additional validation testing was performed by NASA Goddard Space Flight Center [5].

B. Gatefield GF10009 FPGA Testing

The Gatefield 9000 gate FPGA was tested at Texas A&M's cyclotron and Berkeley National Laboratories 88 inch cyclotron. The device was tested to characterize the latchup current for incorporation in a latchup protected device.

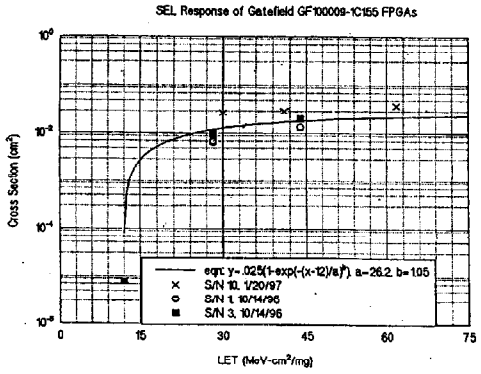


Figure 3. Cross Section vs. LET energy for the Gatefield 9000 gate FPGA.

The latchup cross section versus Linear Energy Transfer (LET) energy is plotted in figure 3. A wide variation in single event related current transients were observed. Typical latchup current was in the range of 300mA to 800mA, however some heavy ion induced current increases were as high as 3.5 A and as low as 50 mA. Test circuit functionality was maintained at the low current levels, however, full FPGA functionality was not monitored. Space Electronics Inc. is currently investigating the heavy ion response and the final design SEL detection threshold has not been set at this time.

V. PRODUCTIZATION

The ADS7805 LPT™ circuit has been developed into a multi-chip module referred to as the 7805RPLP. This device has the same footprint as the ADS7805 with some modification of the pin functions. The separate supplies are replaced by a single VS input. The ADS7805 common supply pin is made available for adding board level decoupling capacitance. The status output replaces the byte input which is internally grounded in the MCM. Care must be taken in the application not to backdrive the device when the status output is active. The latchup current threshold has been set typically at 80 mA with a recovery time of 50 microseconds.

For most space radiation environments, total dose enhancement is required for both the ADS7805 and the LPT™ components, therefore, the 7805RPLP is packaged using SEI's RAD-PAK® packaging technology. This packaging provides shielding of the internal devices from total dose radiation thereby enhancing their total dose hardness.

VI. CONCLUSIONS

Important considerations for the design of latchup protected devices include:

1) Cycling power alone is not sufficient to return the device from a latched state, since the inputs may require current voltage limiting for the latchup protection circuit to work properly.
2) Each device needs to be validated at a heavy ion source to properly set the SEL current detection threshold and properly assess heavy ion response and recovery characteristics.
3) Microlatching can make protecting a circuit more difficult. If the microlatch current is close to the operating current of the device, the LPT™ is not a solution for latchup. If the device is susceptible to microlatch, the microlatch current will need to be characterized for the device.
4) During Single Event Testing (SEE) devices are also susceptible to Total Ionizing Dose (TID). Devices with low TID levels may experience an increase in supply current from the TID. This can also pose a problem for actual space applications. The latchup detection threshold level for these devices must be set at levels consistent with the supply current increase caused by TID.

With proper characterization and design, sensitive devices can be protected at the package level from single event latchups.

Devices which previously were unsuitable for space applications based on their single event latchup threshold characteristics can now be used in a space environment using SEI's LPT™ technology. This technology has been demonstrated for the ADS7805 16 bit analog to digital converter and a product designed for the space environment is available. The application of latchup protection to other devices such as the Gatefield 9000 gate FPGA which exhibit complex SEE effects are being investigated by SEI.

This technology can be applied to a wide range of devices in order to provide new options for the use of commercially developed, leading edge technology components in a space environment.

VII. ACKNOWLEDGMENTS

RAD-PAK® is a registered trademark of Space Electronics Inc.
LPT™ is a trademark of Space Electronics Inc.

This work was partially supported by NASA contract No. NAS8-97186.

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MA31750

Este microprocesador, desarrollado bajo los auspicios de la ESA por GEC PLESSEY en tecnología rad hard (1 Mrad/Si CMOS SOS), implementa la arquitectura definida en la norma MIL-STD-1750. Esta define los elementos básicos de la CPU (unos de obligada implementación y otros opcionales) con el objetivo de establecer un juego de instrucciones para conseguir usar herramientas de desarrollo de software independientes del microprocesador.

La arquitectura definida es de 16 bits en tanto en datos como en direcciones. Por lo tanto el mapa de memoria básico es de 64 Kwords. Opcionalmente puede implementarse una MMU (Memory Management Unit) que extiende la capacidad de direccionamiento a 1 MWord mediante técnicas de paginación.

Se incluye un banco de 16 registros de propósito general y varios de propósito especifico, como el contador de programa, los registros de interrupción pendiente, de mascaras de interrupción, de fallos, de configuración, etc.

Se incorporan muchas características orientadas a soportar sistemas de alta fiabilidad:

- el mapa de I/O está separado, siendo estas instrucciones sólo ejecutadas en modo privilegiado. De hecho los registros de propósito especial, incluidos los de la MMU, son accesibles mediante instrucciones I/O.
- Existen mapas de direcciones separados para instrucciones y operandos.
- el cambio de contexto en interrupciones no esta basado en la pila sino en un sistema de doble vectorización, que proporciona más seguridad en su manejo.
- La MMU proporciona un sistema de protección de acceso a pagina lógicas y/o físicas que permite restringir a cada tarea el acceso a memoria, detectando las posible violaciones.

Existen instrucciones para aritmética punto fijo de hasta 32 bits y punto flotante de hasta 48 bits.

Junto con el procesador, GEC PLESSEY ofrece además de la MMU un dispositivo de detección y corrección de errores (EDAC).

En una aplicación con EDAC trabajando a 13 MHz el throughput obtenido es de 1.25 MIPS.

En la actualidad CRISA tiene desarrollados y calificados varias CPU y ASICs con la "Glue logic" para los computadoras:

- ICE (MIPAS/Envisat)
- ACC (XMM e Integral)
- DPE (Integral), en fase de calificación

Existen otras implementaciones del standard 1750. El PACE1750 es una implementación USA de la que existe versión rad hard. Las diferencias están en las

prestaciones y en la implementación hardware, siendo el software y sus herramientas de desarrollo compatibles.

Se estima que los costes de desarrollo para una CPU PACE 1750 se reducirían sólo a un 30% por el hecho de disponer previamente de sistemas basados en MA31750.

TSC21020E

Este procesador es una versión completamente compatible del ADSP21020 de ANALOG DEVICES realizado por TEMIC con tecnología tolerante a radiación (CMOS 0.8 µm, 50 KRad/Si). La diferencia fundamental reside en que su frecuencia de reloj máxima es del orden 15 MHz, en lugar de los 30 Mhz a los que es capaz de trabajar la versión original. La versión de TEMIC es capaz de proporcionar sobre 15 MIPS y 33 MFLOPS.

Este microprocesador esta basado en una arquitectura Harvard (bancos de memoria y sistema de buses separados para datos y para programa) y se explota en todas sus posibilidades el secuenciamiento (pipelines, caches..) y el paralelismo (multiplicador, ALU y Shift barrel independientes) durante la ejecución. Es una máquina de punto flotante de 40 bits.

Dispone de un banco de 16 registros de propósito general de 40 bits y de varios de propósito especifico que permiten configurar, por ejemplo, decodificación de direcciones (2 bancos en memoria de programa y 4 en datos), el tiempo de acceso a cada banco de memoria, etc. Estas características hacen que necesite muy poca lógica adicional en su implementación.

Su sistema de buses es de 24 bit en direcciones y 32 en datos para la memoria de programa y de 32 bits de direcciones y 40 de datos para el banco de memoria de datos.

Dispone de un juego de instrucciones especializado para tratamiento digital de la señal e incluso de modo de direccionamiento especializados para optimizar operaciones como FFT.

Las herramientas de desarrollo proporcionados por ANALOG DEVICES son un ensamblador y un compilador de leguaje C. A través de un puerto JTAG puede conectarse al sistema de emulación "in circuit" que proporciona ANALOG DEVICES.

En la actualidad, CRISA tiene desarrollado un prototipo de la CPU para la unidad DPU del Instrumento ASCAT (plataforma Metop).

80C86

Este procesador en la versión CMOS del conocido y casi obsoleto standard comercial. En la actualidad HARRIS lo fabrica todavía en versiones con grado de calificación militar. También siguen disponible varios de sus periféricos (UART, PIC, DMA....).

Este procesador esta basado en una arquitectura de punto fijo de 16 bits, presentando en esta versión un bus de datos y direcciones multiplexado de 16/20 bits. Su espacio de direccionamiento es un Mbyte y utiliza técnicas de segmentación.

Existen versiones que corren hasta 8 MHz proporcionando un throughput de hasta 1 MIPS.

Existen numerosas herramientas de desarrollo comerciales.

La principal característica de los desarrollos basados en 8086 es su bajo coste debido a la amplia experiencia existente en el mundo comercial.

CRISA desarrollo una CPU basada en 80186 para el experimento EDMO, que llevo a cabo su misión en Septiembre 1994 a bordo del STS64 (Space Shuttle). Este procesador es una versión del anterior, que incorpora algunos periféricos como UART y TIMERS.

ERC32

El ERC32 es un procesador multi-chip desarrollado por TEMIC con el soporte de la Agencia Espacial Europea (ESA) con tecnología CMOS 0.8 µm tolerante a radiación (mayor que 50 Krads (Si)). Está basado en la arquitectura SPARC V7 (procesador RISC de buses de datos y direcciones de 32 bits) y se compone fundamentalmente de tres componentes: una unidad de punto entero (Integer Unit, IU), una unidad de punto flotante (Floating point unit, FPU) y una unidad controladora de memoria (Memory Controller, MEC).

Las unidad de punto entero (IU) y de punto flotante (FPU) están basadas en los dispositivos 90C601 y 90C602 de MHS respectivamente. La unidad controladora de memoria (MEC) es un ASIC que inplementa el interface del núcleo procesador con la memoria y unidades de E/S y que contiene funciones de soporte adicionales, como watchdog, EDAC, dos UARTS, timers, etc.

En todas las unidades que componen el núcleo básico, se han incorporado funciones de soporte y detección de errores concurrentes con alto grado de cobertura (más del 99 % de errores inducidos por SEU son detectados).para hacer del ERC32 un núcleo de cálculo fiable, por lo que hace que éste tipo de sistemas sean adecuados para aplicaciones militares y espaciales.

El sistema implementa el juego de instrucciones SPARC versión 7 y está diseñado para obtener un nivel de procesamiento de 10 MIPS para la unidad de punto entero en paralelo con 2 MFLOPS para la unidad de punto flotante a una frecuencia de trabajo de 14 MHz.

En la actualidad, existe un proyecto interno en CRISA de desarrollo de un computador basado en el núcleo ERC32. El prototipo estará disponible a finales de 1997.

Subject: **Re: Descripcion de microprocesadores**
Date: Tue, 11 Nov 1997 13:03:00 -0100
From: Jose Miguel Herreros <jhl@ll.iac.es>
Organization: I.A.C.
To: "F. Peran" <fperan@crisa.es>
CC: Jose Miguel Herreros <jhl@ll.iac.es>, "Javier G. Huete" <jhuete@crisa.es>, "Jose. Moreno" <moreno@crisa.es>, Fleming Pedersen <pedersen@crisa.es>

Estimado Paco,

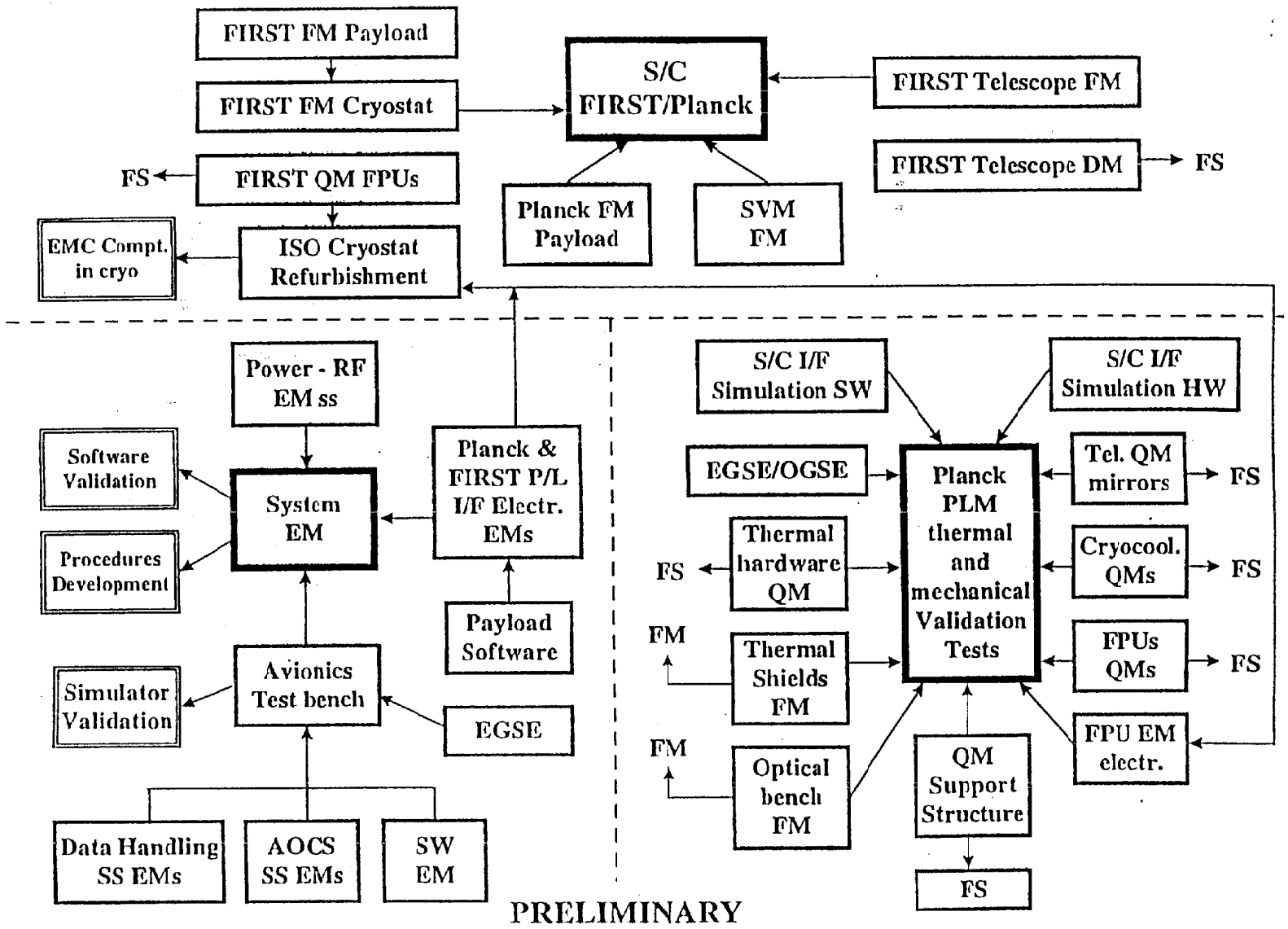
Muchas gracias por tu información relativa a micros para el espacio.

Ayer estuve revisando la informacion que tengo disponible de SOHO relativa a microprocesadores, mi única referencia. La mayoria utilizó el 80C86. Por otra parte MMS empleó en el satélite el MAS281, de 16 bits, por lo visto desarrollado por Marconi y que cumple el standard MIL-STD-1750A. Curiosamente Alcatel que partipó en uno de los intrumentos, bajo contrato de la Universidad de Alcalá de Henares, también utilizó este mismo micro. Otro instrumento utilizó uno de 32 bits, el Sandia Lab SA3000, parece ser que es equivalente al 32C016 de National Semiconductors.

Sabes algo del MAS281?.

Sin otro particular,
Recibe un cordial saludo.
Jose.

Jose Miguel Herreros Linares	fax:	34-(9)22 605210
Instituto de Astrofisica de Canarias	Institute phone:	34-(9)22 605200
c/ Via Lactea s/n	Secretary phone:	34-(9)22 605360
38200 La Laguna	Office phone	34-(9)22 605358
Tenerife. Spain	e-mail:	jhl@iac.es


FIRST FM Payload
FIRST FM Cryostat
S/C FIRST/Planck
FIRST Telescope FM
FIRST Telescope DM
FS
FS
FIRST QM FPUs
Planck FM Payload
SVM FM
EMC Compt. in cryo
ISO Cryostat Refurbishment
Power - RF EM ss
S/C I/F Simulation SW
S/C I/F Simulation HW
Software Validation
System EM
Planck & FIRST P/L I/F Electr. EMs
EGSE/OGSE
Planck PLM thermal and mechanical Validation Tests
Tel. QM mirrors
FS
Procedures Development
Thermal hardware QM
FS
Cryocool. QMs
FS
Payload Software
FM
Thermal Shields FM
FPUs QMs
FS
Simulator Validation
Avionics Test bench
EGSE
FM
Optical bench FM
QM Support Structure
FPU EM electr.
Data Handling SS EMs
AOCS SS EMs
SW EM
FS
PRELIMINARY

```
          SHUTTER_L     (3)                                          F
          END_SEQ_NOP   (160)                                        F
          SHUTTER_L     (0)                                          F
          END_SEQ_NOP   (160)                                        F
          END_ICS
ICSDURTN = T
-------------------------------------------------------------------------
ICSNAME  = SF0871
ICSDESC  = CCE SHORT FUNCTIONAL TEST - PART 1
          ICSNAME       SF0871
          LABEL         CCE SHORT FUNCTIONAL TEST - PART 1
          END_SEQ_NOP   (0)                                          F
          POWER_ADC_L   (2)                                          F
          TM_16KBPS_L   (44)                                         F
          HEATERS_SW_L  (45)                                         F
          HEATERS_LW_L  (204)                                        F
          BIAS_B1_B2_L  (9)                                          F
          BIAS_B3_B4_L  (36)                                         F
          BIAS_B5_B6_H  (36)                                         F
          GAIN_B1_L     (1)                                          F
          GAIN_B2_L     (1)                                          F
          GAIN_B3_L     (1)                                          F
          GAIN_B4_L     (1)                                          F
          GAIN_B5_L     (1)                                          F
          GAIN_B6_L     (1)                                          F
          GAIN_HK_L     (1)                                          F
          MODE_HK_L     (1)                                          F
          RUN_FLAGS_L   (0)                                          F
          SW_RST_INT    (32)                                         F
          SW_RST_LEN    (2)                                          F
          LW_RST_INT    (32)                                         F
          LW_RST_LEN    (2)                                          F
          RUN_FLAGS_L   (12)                                         F
          SHUTTER_L     (2)                                          F
          SHUT_CS_1_L   (40)                                         F
          SHUT_CS_2_L   (40)                                         F
          HEADER_5_L    (0)                                          F
          SWSC_DNPOS    (2047)                                       F
          HEADER_6_L    (0)                                          F
          LWSC_DNPOS    (2047)                                       F
          HEADER_7_L    (52)                                         F
          FP_DN_MATN    (1024)                                       F
          FP_DN_COR1    (1024)                                       F
          FP_DN_COR2    (1024)                                       F
          END_ICS
ICSDURTN = T
-------------------------------------------------------------------------
ICSNAME  = SF0872
ICSDESC  = CCE SHORT FUNCTIONAL TEST - PART 2
          ICSNAME       SF0872
          LABEL         CCE SHORT FUNCTIONAL TEST - PART 2
          END_SEQ_NOP   (0)                                          F
          POWER_ADC_L   (2)                                          F
          TM_16KBPS_L   (44)                                         F
          HEATERS_SW_L  (63)                                         F
          HEATERS_LW_L  (255)                                        F
          BIAS_B1_B2_L  (15)                                         F
```

```
AUTHOR   = O.H. BAUER, M. STEINMAYER/MPE - C.v.DIJKHUIZEN, M.v.d.LINDEN/SRU
TOTNICS  = 1
ICSNAME  = SF4900
ICSDESC  = SHUTTER CONTROL
        ICSNAME      SF4900
        LABEL        SHUTTER CONTROL
        SHUTTER_L    (*)                                    A SF4900-01
        END_ICS
ICSDURTN = T
RANGES   = 1
SF4900-01= SHUTTER POSITION 0, 1, 2 OR 3
```

```
ICS-FILE SF50.ICS VERSION 2.0
FILENAME = SF50.ICS
DATE     = 91/06/14
AUTHOR   = O.H. BAUER, M. STEINMAYER/MPE - C.v.DIJKHUIZEN, M.v.d.LINDEN/SRU
TOTNICS  = 1
ICSNAME  = SF5000
ICSDESC  = SW SCANNER PARAMETER SET-UP
        ICSNAME      SF5000
        LABEL        SW SCANNER PARAMETER SET-UP
        SWSC_STPOS   (*)                                    A SF5000-01
        SWSC_NSTPP   (*)                                    A SF5000-02
        SWSC_STSZP   (*)                                    A SF5000-03
        SWSC_STINP   (*)                                    A SF5000-04
        SWSC_NSTPN   (*)                                    A SF5000-05
        SWSC_STSZN   (*)                                    A SF5000-06
        SWSC_STINN   (*)                                    A SF5000-07
        SWSC_NSCAN   (*)                                    A SF5000-08
        END_ICS
ICSDURTN = T
RANGES   = 8
SF5000-01= Scanner start position:              Range 0 to 8190
SF5000-02= Number of positive scan steps:       Range 0 to 65535
SF5000-03= Scanner positive step size:          Range 0 to 65535
SF5000-04= Scanner positive step interval:      Range 0 to 65535
SF5000-05= Number of negative scan steps:       Range 0 to 65535
SF5000-06= Scanner negative step size:          Range 0 to 65535
SF5000-07= Scanner negative step interval:      Range 0 to 65535
SF5000-08= Number of scans:                     Range 0 to 65535
```

```
ICS-FILE SF51.ICS VERSION 2.0
FILENAME = SF51.ICS
DATE     = 91/06/14
AUTHOR   = O.H. BAUER, M. STEINMAYER/MPE - C.v.DIJKHUIZEN, M.v.d.LINDEN/SRU
TOTNICS  = 1
ICSNAME  = SF5100
ICSDESC  = SW SCANNER HEADER SET-UP
        ICSNAME      SF5100
        LABEL        SW SCANNER HEADER SET-UP
        HEADER_5_L   (*)                                    A SF5100-01
        END_ICS
ICSDURTN = T
RANGES   = 1
SF5100-01= Header setting: (0-255)
```

```
S_GCAL_HI
SW_RST_INT    (16)
LW_RST_INT    (16)
HEADER_5_L    (128)
SWSC_STPOS    (3910)
SWSC_NSTPP    (92)
SWSC_STSZP    (2)
SWSC_STINP    (16)
SWSC_NSTPN    (0)
SWSC_STSZN    (0)
SWSC_STINN    (0)
SWSC_NSCAN    (1)
HEADER_6_L    (128)
LWSC_STPOS    (3910)
LWSC_NSTPP    (92)
LWSC_STSZP    (2)
LWSC_STINP    (16)
LWSC_NSTPN    (0)
LWSC_STSZN    (0)
LWSC_STINN    (0)
LWSC_NSCAN    (1)
INTERVAL      (1456)
SHUT_CS_1     (CS_GRATNG_HI)
SHUT_CS_1     (CS_GRATNG_ON)
RUN_FLAGS_L   (124)
END_PCS

S_CURE_FLUSH
INTERVAL      (4000)
SHUT_CS_1     (FLUSH_SRC_HI)
SHUT_CS_1     (FLUSH_SRC_ON)
SYNC_FLAG     (SET)
RUN_FLAGS_L   (28)
END_PCS
```

Instrument Operating Modes:

Primary: One or more Primary modes.
Science and HK data are produced at a rate compatible with the OBDH, as defined in the IID-B.

Serendipity: One of the Primary modes which could be used during FIRST slews.
Science and HK data are produced at a rate compatible with the OBDH, as defined in the IID-B.

Partner: Two instruments both operating in one of their Primary modes.
Science and HK data are produced by the two instruments at a rate compatible with the OBDH, as defined in the IID-B's.

Standby: A 'warm-up' mode from which an instrument is ready to start observations in one of its Primary modes.
HK data only is produced at a rate compatible with the OBDH, as defined in the IID-B.

Sleep: A mode in which the instrument is partly active. It could be used when another instrument is in Primary mode, or as a predecessor to Standby mode.
HK data only is produced at a rate compatible with the OBDH, as defined in the IID-B.

Off: A mode in which all power is removed from the instrument.
The instrument produces no data through its telemetry interface, but limited temperature data are available from Spacecraft powered sensors (TBC)

Test: Not really an operating mode, but any possible instrument configuration, within the allowed resources, to allow functional and performance testing as well as investigations of fault conditions.

The transition between the different modes are depicted in ***Figure 2*** *and* ***Figure 3***.

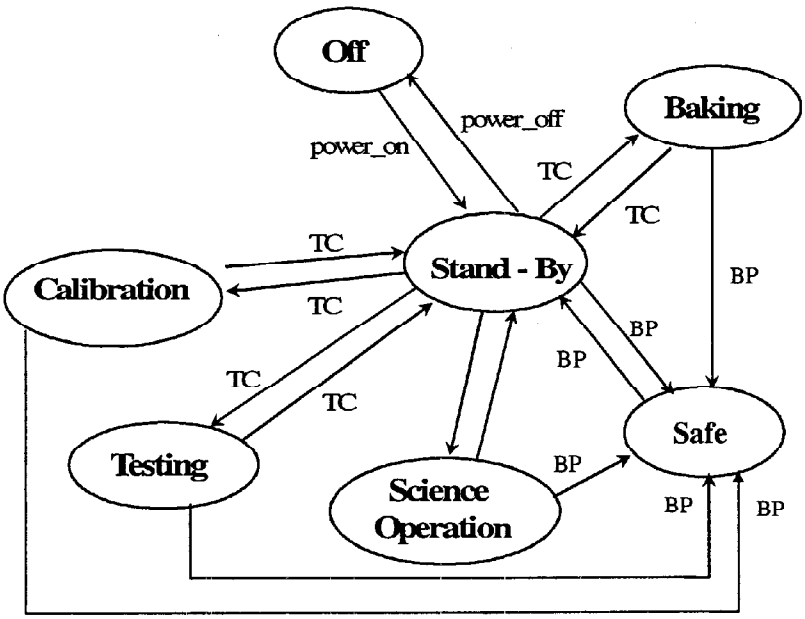
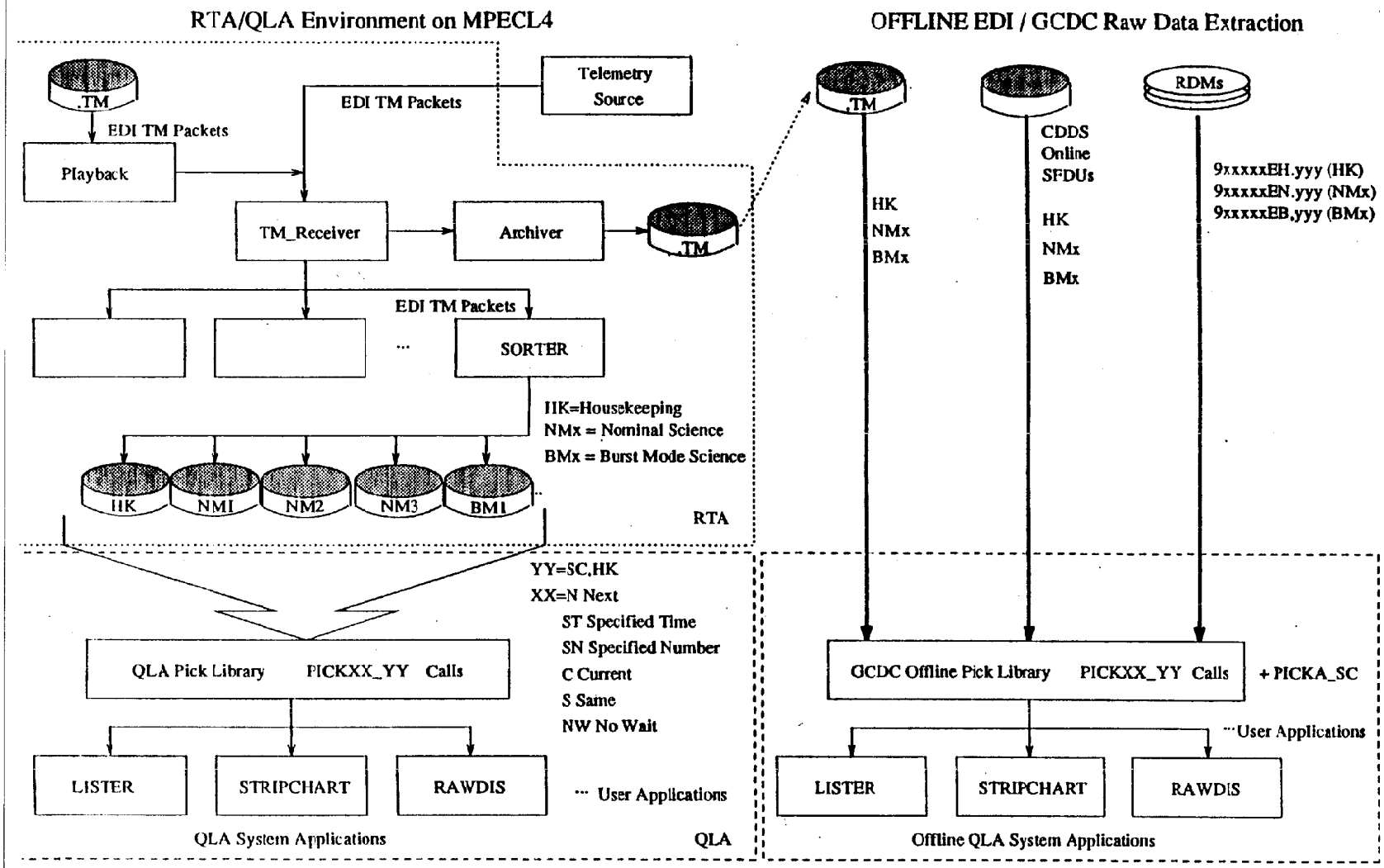
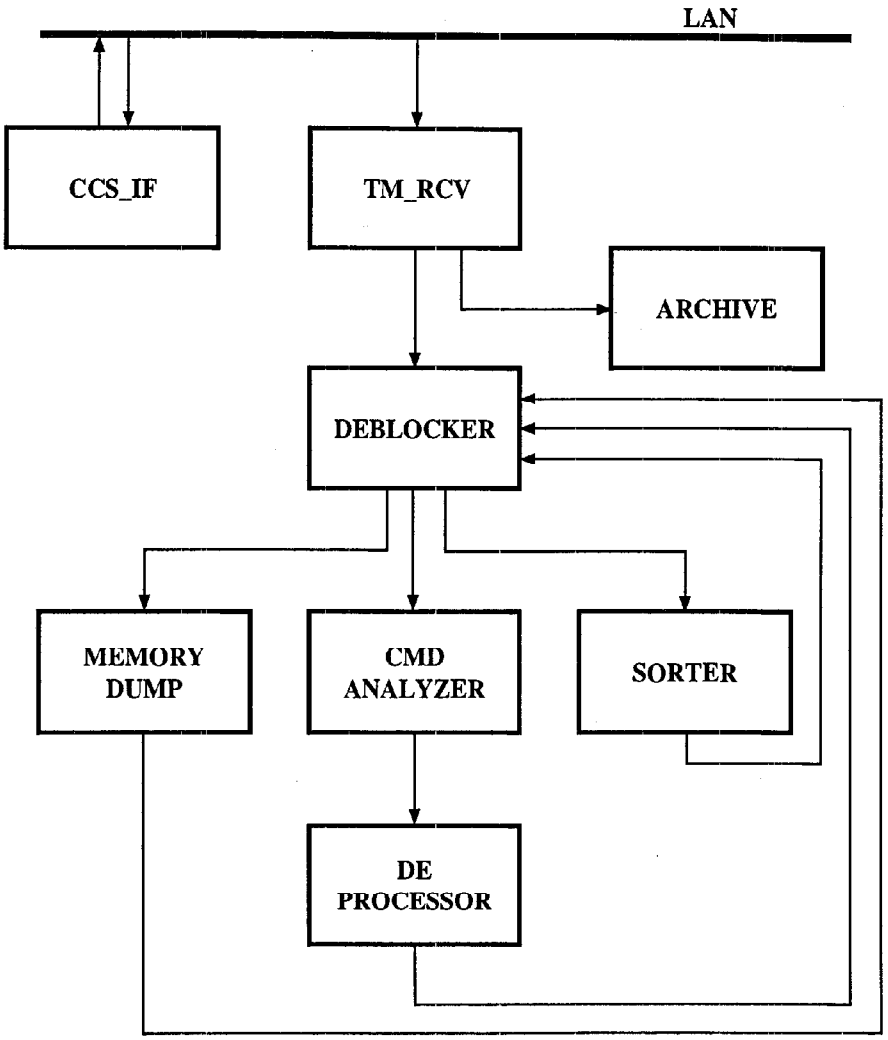
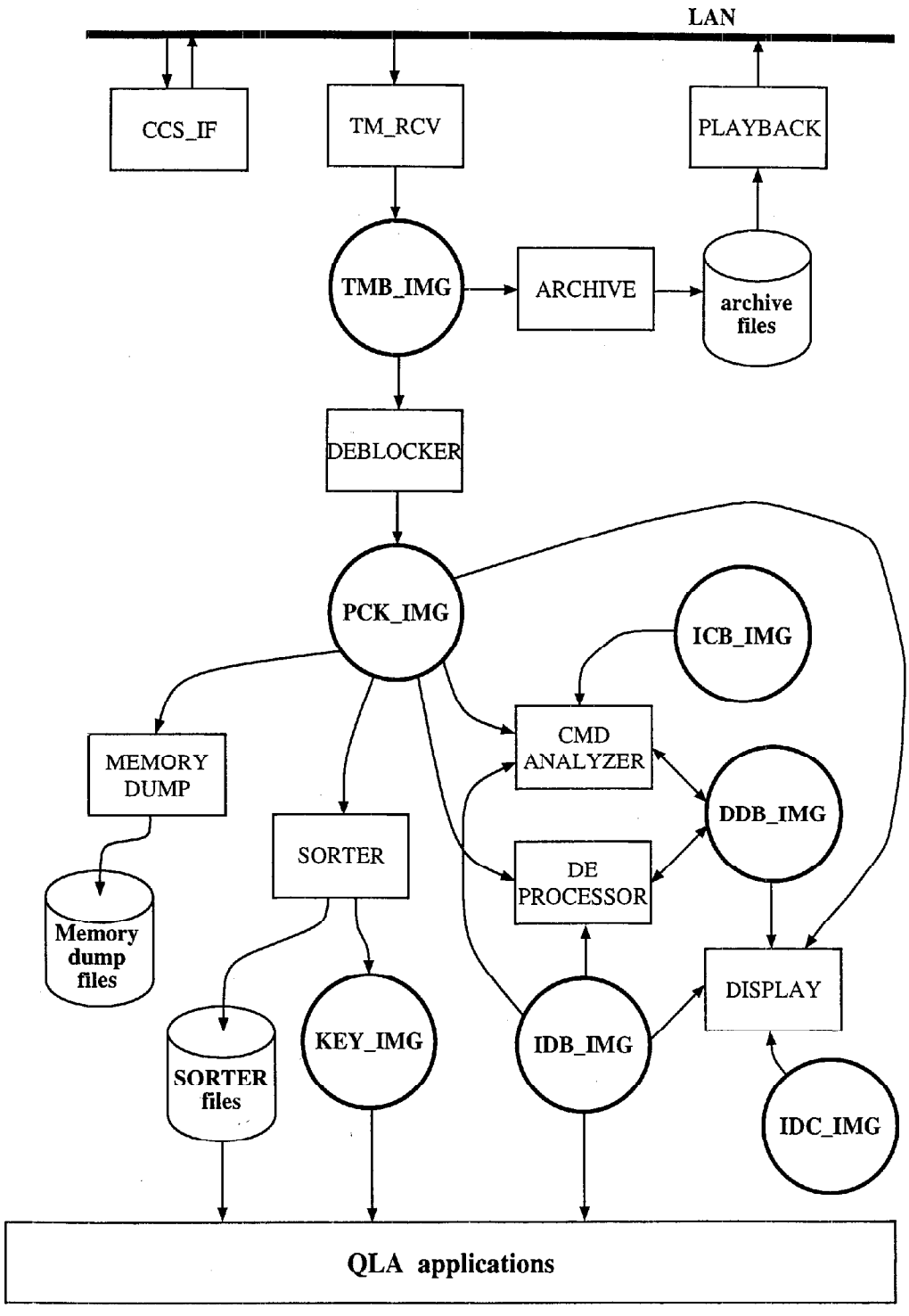


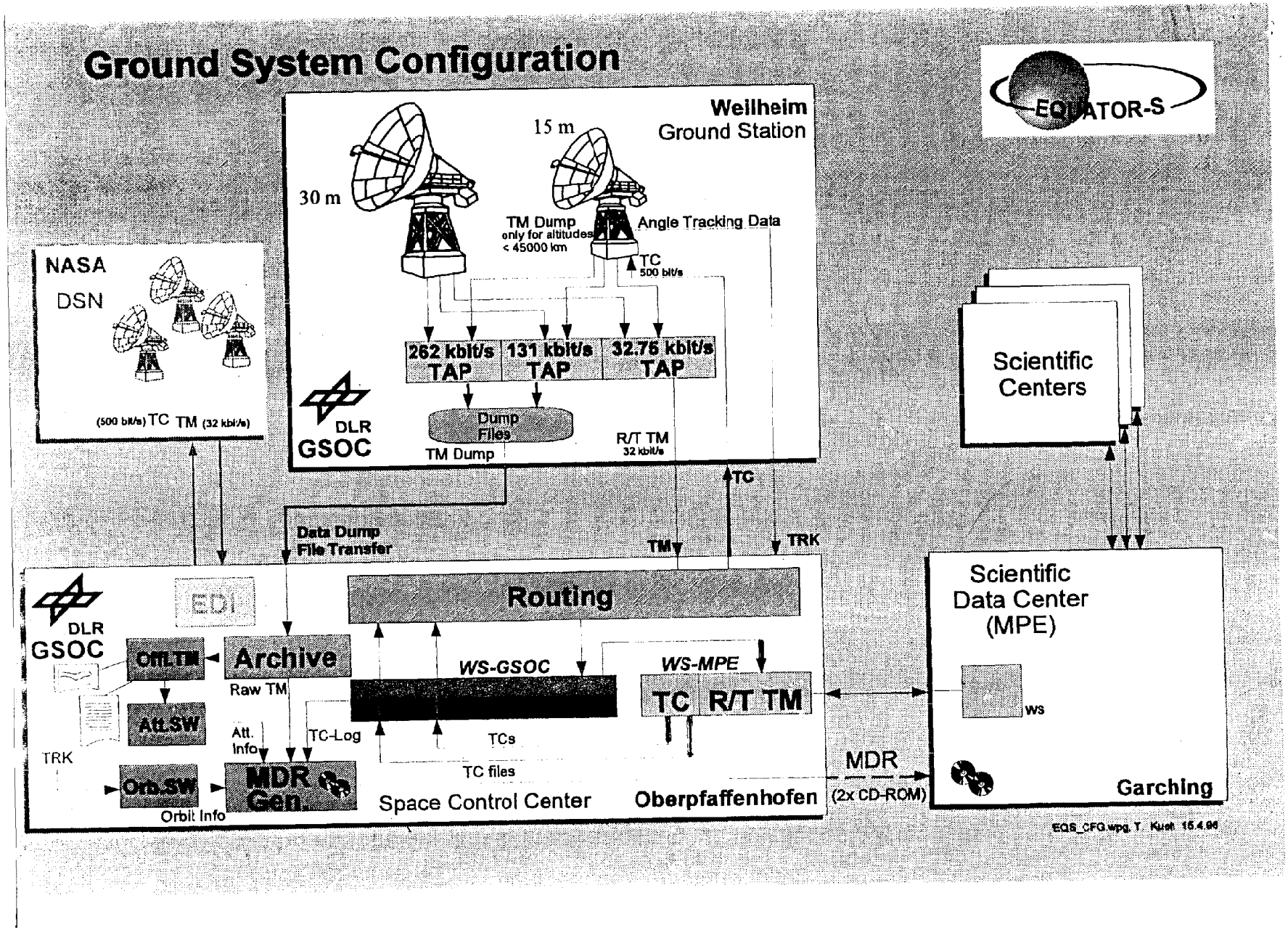
Figure 2: Top Level Mode Changes Diagram


RTA/QLA Environment on MPECL4
OFFLINE EDI / GCDC Raw Data Extraction
.TM
EDI TM Packets
Telemetry Source
Playback
TM_Receiver
Archiver
SORTER
HK=Housekeeping
NMx = Nominal Science
BMx = Burst Mode Science
HK
NM1
NM2
NM3
BM1
RTA
YY=SC,HK
XX=N Next
ST Specified Time
SN Specified Number
C Current
S Same
NW No Wait
QLA Pick Library PICKXX_YY Calls
LISTER
STRIPCHART
RAWDIS
User Applications
QLA System Applications
QLA
HK
NMx
BMx
CDDS
Online
SFDUs
RDMs
9xxxxxEH.yyy (HK)
9xxxxxEN.yyy (NMx)
9xxxxxEB,yyy (BMx)
GCDC Offline Pick Library PICKXX_YY Calls
+ PICKA_SC
User Applications
Offline QLA System Applications


LAN
CCS_IF
TM_RCV
ARCHIVE
DEBLOCKER
MEMORY DUMP
CMD ANALYZER
SORTER
DE PROCESSOR


LAN
CCS_IF
TM_RCV
PLAYBACK
TMB_IMG
ARCHIVE
archive files
DEBLOCKER
PCK_IMG
ICB_IMG
CMD ANALYZER
MEMORY DUMP
DDB_IMG
SORTER
DE PROCESSOR
Memory dump files
DISPLAY
KEY_IMG
IDB_IMG
SORTER files
IDC_IMG
QLA applications

```
$! FILE TPF_63.COM
$! AUTHOR M. STEINMAYER -MPE- / Rev. C.v.Dijkhuizen -SRON/SRU-
$! DATE 14-MAY-1990
$! REVISION DATE 14-JUNE-1991
$! VERSION 2.1
$!*****************************************************************!$
$!                                                                 !$
$! TPF63 : DETECTOR SIGNAL QUALITY AND THERMAL SELF-EMISSION       !$
$!                                                                 !$
$! SVS-T02.2.5                                                     !$
$!                                                                 !$
$!*****************************************************************!$
$!
$!
$ TP_START_PROC TPF63 "DETECTOR SIGNAL QUALITY AND THERMAL SELF-EMISSION"
$!
$!
$ CNT_HTRS   = 1
$ CNT_BIAS   = 1
$ CNT_RESET  = 1
$ CNT_DIFCAL = 1
$ CNT_GAIN   = 1
$ CNT_STABIL = 1
$ CNT_FP_CUR = 1
$ CNT_SC_CUR = 1
$!
$!
$!
$ HTR_LOOP:  !---------------------- DETECTOR HEATER LOOP ------------------
$!
$ IF CNT_HTRS.EQ.1               !            B1/B2    B3/B4     B5/B6
$ THEN
$ TP_CALL_ICS SF9400 "36 136"    !  OFF        OFF    LEVEL 0   LEVEL 0
$ ENDIF
$ IF CNT_HTRS.EQ.2
$ THEN
$ TP_CALL_ICS SF9400 "45 204"    !  NOMINAL    LOW    LEVEL 4   LEVEL 4
$ ENDIF
$!
$ BIAS_LOOP:  !--------------------- BIAS LOOP ---------------------------
$!
$ IF CNT_BIAS.EQ.1               !            B1/B2    B3/B4     B5/B6
$ THEN
$ TP_CALL_ICS SF9700 "2 9 9"     !  0.6 X   OFF/LVL1  LEVEL 1   LEVEL 1
$ ENDIF
$ IF CNT_BIAS.EQ.2
$ THEN
$ TP_CALL_ICS SF9700 "12 36 36"  !  1.0 X   OFF/LVL6  LEVEL 4   LEVEL 4
$ ENDIF
$ IF CNT_BIAS.EQ.3
$ THEN
$ TP_CALL_ICS SF9700 "8 45 45"   !  1.2 X   OFF/LVL4  LEVEL 5   LEVEL 5
$ ENDIF
$!
$ TP_WAIT 00:10:00
$!
$ RESET_LOOP:  !-------------------- RESET LOOP ----------------------
$!
$ IF CNT_RESET.EQ.1
$ THEN
$ TP_CALL_ICS SF8300 "16 16"     !  RESET INTERVALS  1 SECOND
$ ENDIF
$ IF CNT_RESET.EQ.2
$ THEN
$ TP_CALL_ICS SF8300 "160 160"   !  RESET INTERVALS 10 SECONDS
$ ENDIF
$!
$ DIFCAL_LOOP:!---------------- DIFFUSE CALIBRATOR LOOP -----------
$!
$ IF CNT_DIFCAL.EQ.1
$ THEN
$ TP_CALL_ICS SF4700 "CS_DIFFUS_LO CS_DIFFUS_ON"   !   LOW
$ ENDIF
$ IF CNT_DIFCAL.EQ.2
$ THEN
$ TP_CALL_ICS SF4700 "CS_DIFFUS_HI CS_DIFFUS_ON"   !   HIGH
$ ENDIF
$!
$ GAIN_LOOP:  !----------------- GAIN LOOP ---------------------
$!
$ IF CNT_GAIN.EQ.1
$ THEN
$ TP_CALL_ICS SF9100 "0 0 0 0 0 0"   !      1 X
$ ENDIF
$ IF CNT_GAIN.EQ.2
$ THEN
$ TP_CALL_ICS SF9100 "1 1 1 1 1 1"   !      4 X
$ ENDIF
$ IF CNT_GAIN.EQ.3
$ THEN
$ TP_CALL_ICS SF9100 "2 2 2 2 2 2"   !     16 X
$ ENDIF
$!
$ IF CNT_RESET.EQ.1
$ THEN
$ WAIT 00:00:20                      !   20 RESET INTERVALS
$ ENDIF
$!
$ IF CNT_RESET.EQ.2
$ THEN
$ WAIT 00:03:20                      !   20 RESET INTERVALS
$ ENDIF
```


Ground System Configuration
EQUATOR-S
Weilheim
Ground Station
30 m
15 m
TM Dump
only for altitudes
< 45000 km
Angle Tracking Data
TC
500 bit/s
NASA
DSN
(500 bit/s) TC TM (32 kbit/s)
262 kbit/s
TAP
131 kbit/s
TAP
32.75 kbit/s
TAP
DLR
GSOC
Dump
Files
TM Dump
R/T TM
32 kbit/s
Scientific
Centers
TC
TRK
Data Dump
File Transfer
TM
DLR
GSOC
EDI
Routing
OrbTM
Archive
Raw TM
WS-GSOC
WS-MPE
TC R/T TM
Scientific
Data Center
(MPE)
WS
AttSW
Att.
Info
TC-Log
TCs
TRK
TC files
MDR
(2x CD-ROM)
OrbSW
MDR
Gen.
Orbit Info
Space Control Center
Oberpfaffenhofen
Garching
EQS_CFG.wpg, T. Kuse 15.4.96

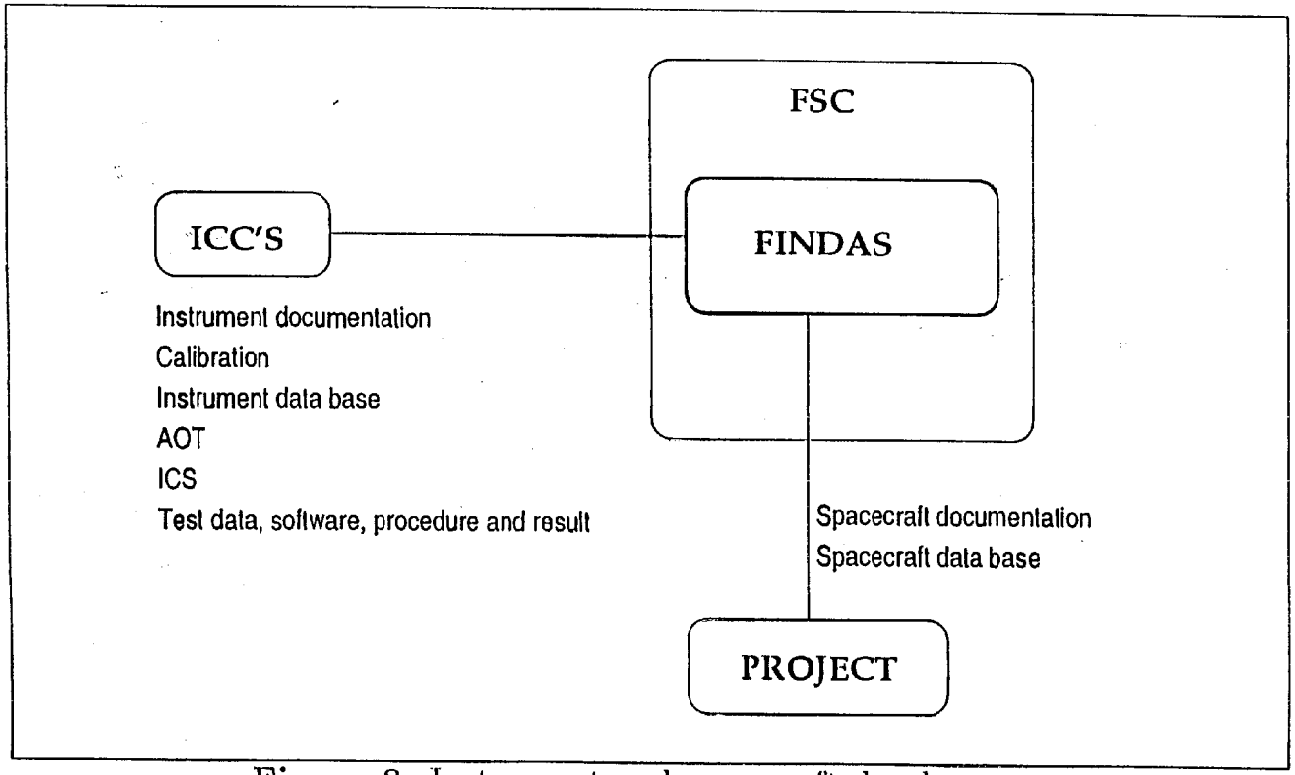


Figure 8: Instrument and spacecraft development

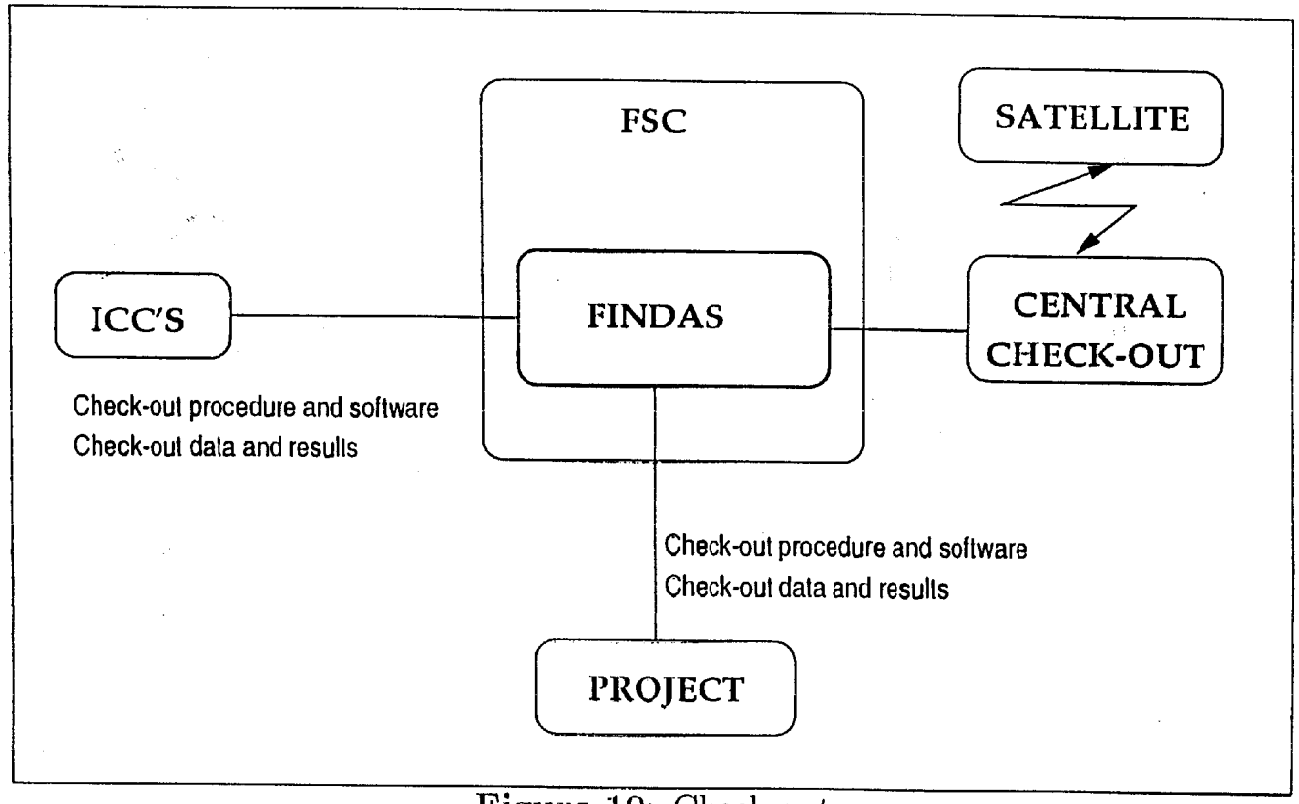


Figure 10: Check-out

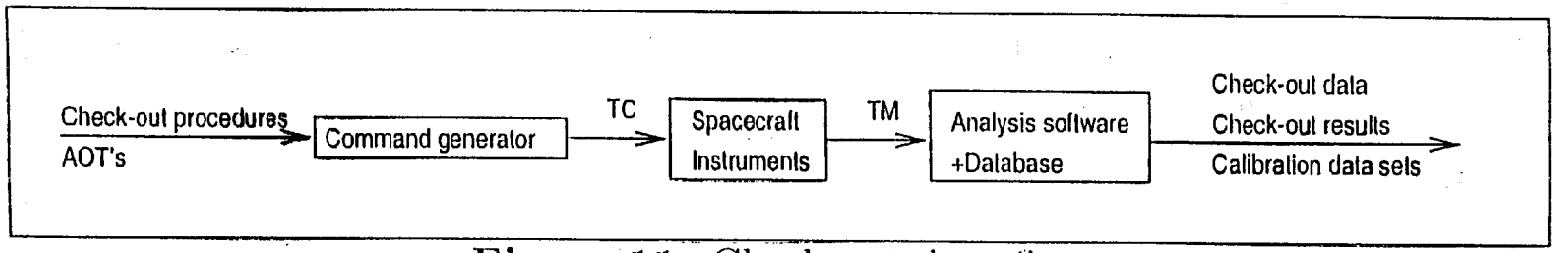


Figure 11: Check-out data flow

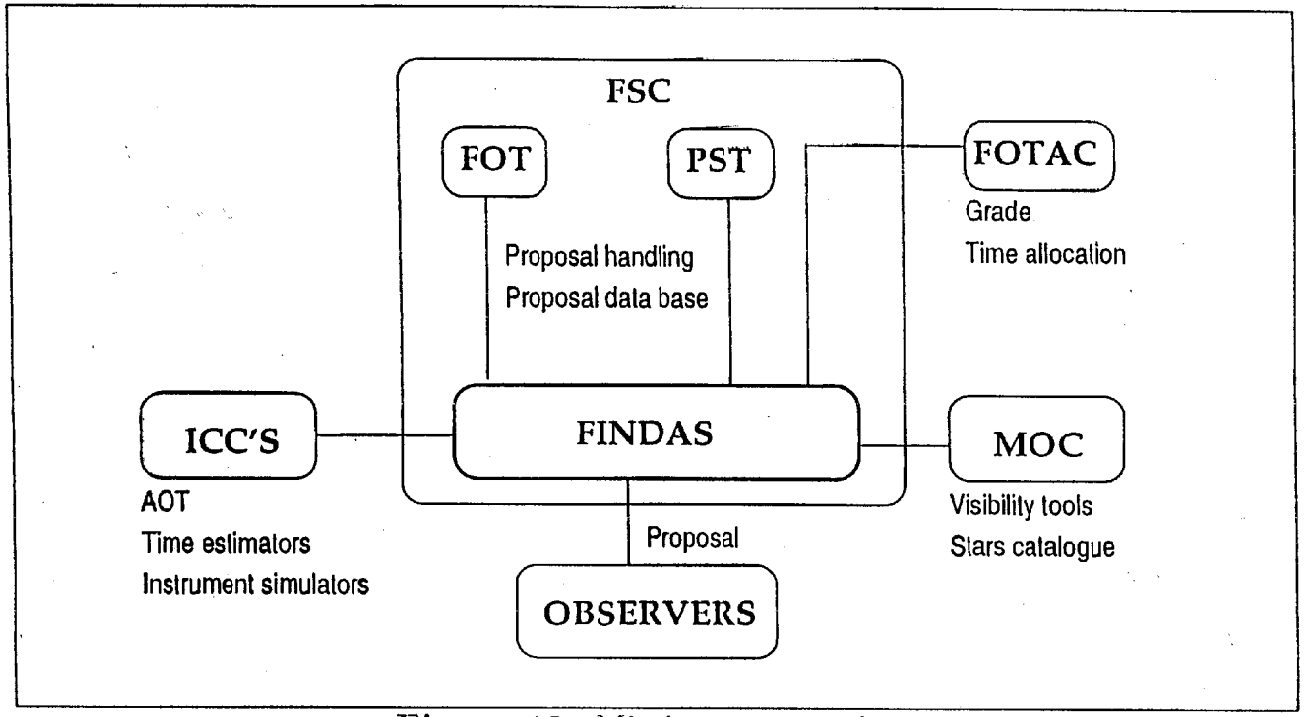


Figure 12: Mission preparations

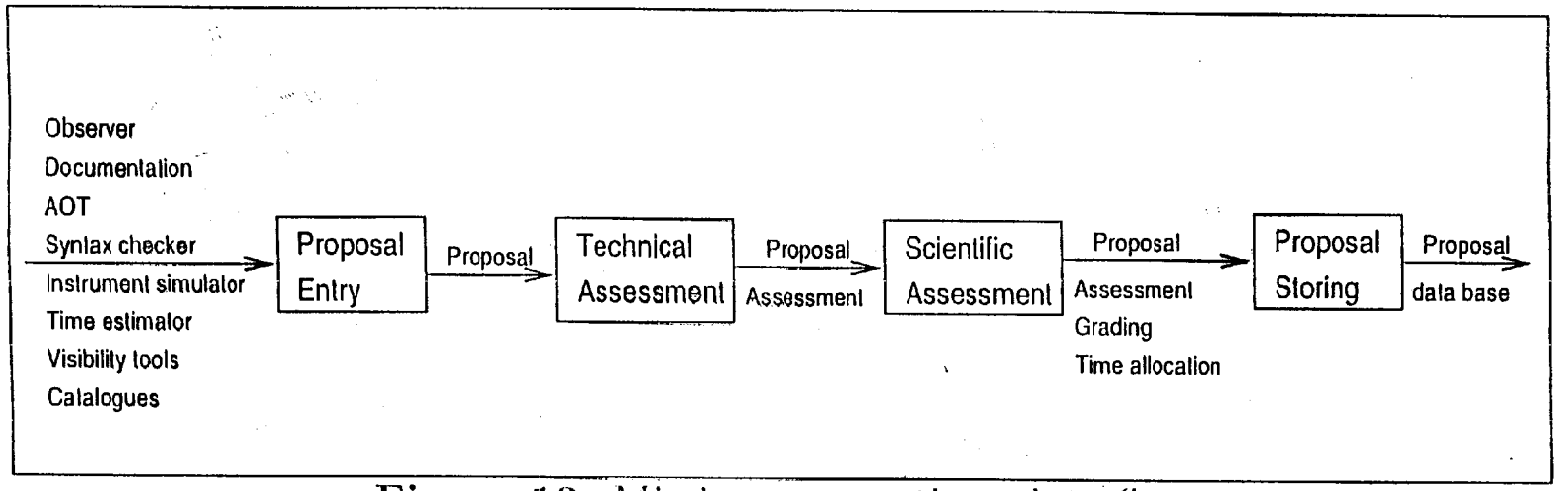


Figure 13: Mission preparations data flow

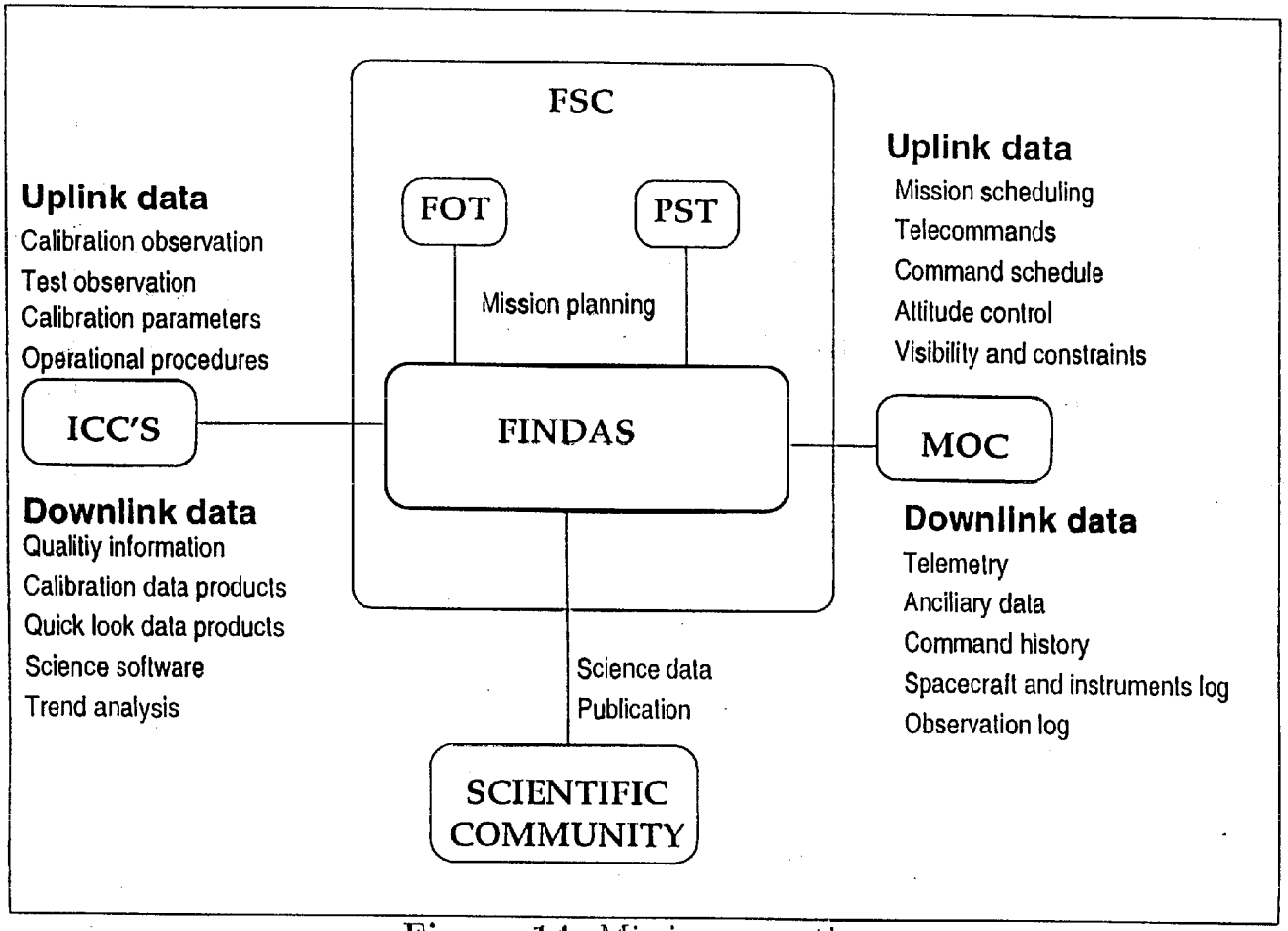


Figure 14: Mission operations

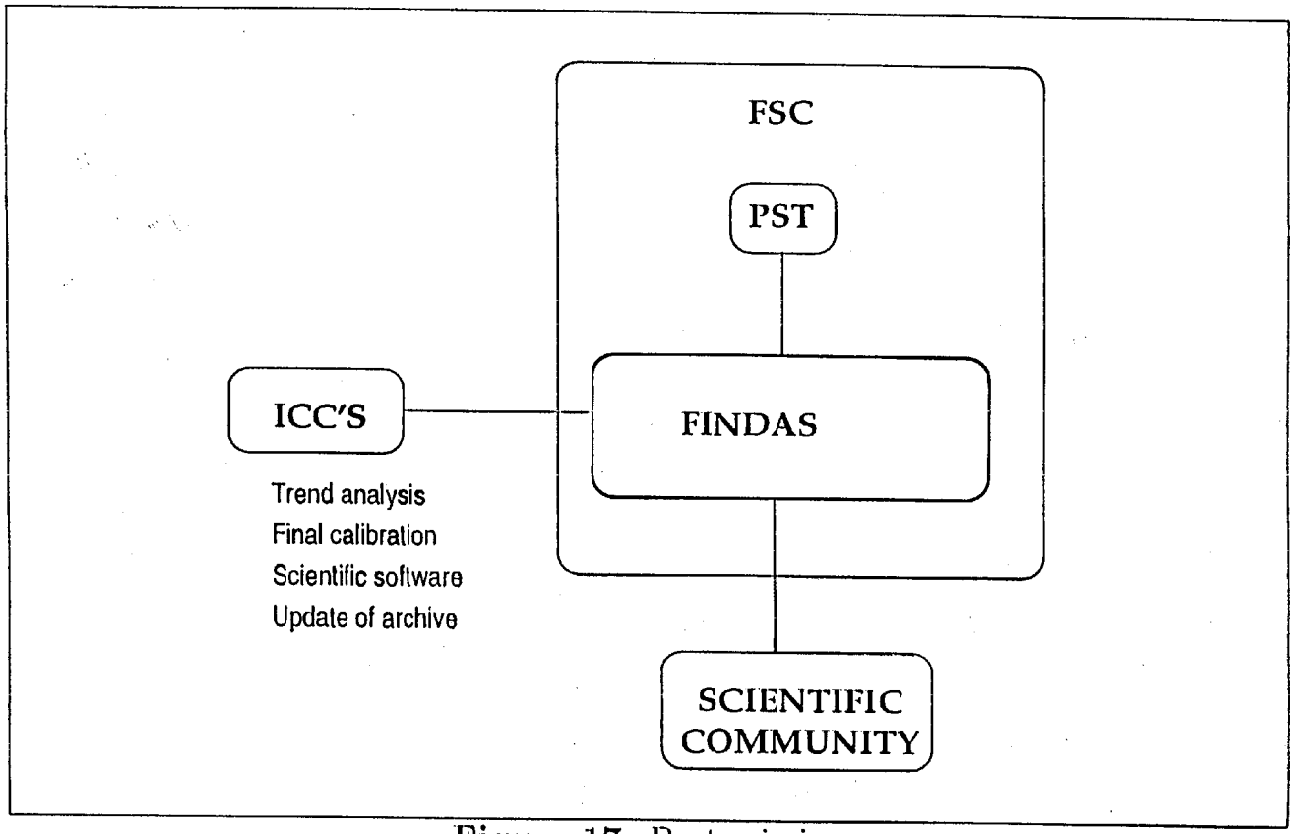


Figure 17: Post mission

esa

FIRST

Very modern archive = objects + relations + methods