

-----Original Message-----

From: Matt Griffin <M.J.Griffin@qmw.ac.uk>
To: Bruce Swinyard <b.m.swinyard@rl.ac.uk>; Ken King <k.j.king@rl.ac.uk>
Date: 11 December 1998 13:47
Subject: SPIRE electronics (fwd)

>
>
>----- Forwarded message -----
>Date: Thu, 10 Dec 1998 21:42:40 -0800 (PST)
>From: James Bock <jjb@astro.caltech.edu>
>To: matt griffin <M.J.Griffin@qmw.ac.uk>
>Cc: Viktor Hristov <vvh@phobos.caltech.edu>,
> colin cunningham <c.cunningham@roe.ac.uk>
>Subject: SPIRE electronics

>
>
>Hi Matt,

>
>I am faxing you a candidate circuit for the warm electronics.
>I think you will see that low-power designs are possible, but
>require some complexity. The preamp, built from discrete
>components, dissipates 53 mW/channel. Two possible 16-bit A/D
>converters are the ADS7807 (planned for the HF1) at 35mW max
>dissipation, and the 7809LPRP (rad hard, latchup protected) at
>132 mW max dissipation. In the latter case especially we could
>multiplex several channels onto a single A/D with an analog MUX
>before the A/D converter. An 18-bit A/D would reduce the sampling
>rate (see below), but may have further qualification issues with
>ESA?

>
>Total power, with a single ADS7807 per channel, is 88 mW/channel,
>or 53 W for 600 channels. Of course this does not include the other
>electronics we will need (voltage regulators, AC bias supply,
>possibly a few channels for temperature control). The expected noise
>performance of the preamp is quite good - 3nV/rtHz - including a
>10 kOhm output impedance from the JFETs.

>
>I think it is fair to say that there was general concern about the
>total power budget available for the warm electronics, and the
>components that would be allowed to fly, at the last bolometer
>meeting. So naturally we are very interested in the reaction the
>component and power issues.

>
>The SPU will be required to perform demodulation of the signals.
>The sampling rate of the A/D converters is determined by the total
>voltage across the bolometers, the detector noise, and the noise on
>the A/D converter:

>
> $2.8 \cdot V_{rms} / [V_n \cdot \sqrt{B}] < (1/2) \cdot 2^N,$

>
>where N is the number of bits to the noise level. Assuming N = 15,
> $V_n = 20 \text{ nV/rtHz}$, $V_{rms} = 7 \text{ mV}$ implies $B = 3.5 \text{ kHz}$ and a sampling rate
>of 7 kHz. The resulting data rate into the SPU is then $2^7 \cdot 600$
>= 8 MB/s. This is probably a bit of an overestimate - I'll have to

>calculate for each waveband separately. Using an 18 bit converter,
>for example, would slow the data rate into the SPU by a factor of 16.
>Naturally the demodulated data rate post SPU is much slower.

>
>Finally, we are also concerned about the interface to the shell of
>the dewar for the cables going to the warm electronics. At a minimum
>we would like to have the RF-tight connection we mentioned earlier
>with rigid attachment of the cables to the inside of the fixture.
>Depending on the RF shielding architecture, we may wish to put
>passive RF filters here, or at the 15K shield. Do you have any
>numbers for parasitic power dissipation onto the dewar shell?

>
>On other issues, we are making good progress on the focal plane
>design. When do you think a mechanical envelope will be available?
>It would definitely help guide our work. Also it would be very
>valuable to have the 350um feedhorn array measured at QMW. What
>are the prospects for doing that in the next month or so? I am
>worried that the prototype may have some problems at the waveguide
>section on 2 of the 7 horns. Marty is working to fix these problems,
>incurred during machining of the mandrels, but it would be a bit
>scary to order the test feedhorn arrays without measurements.

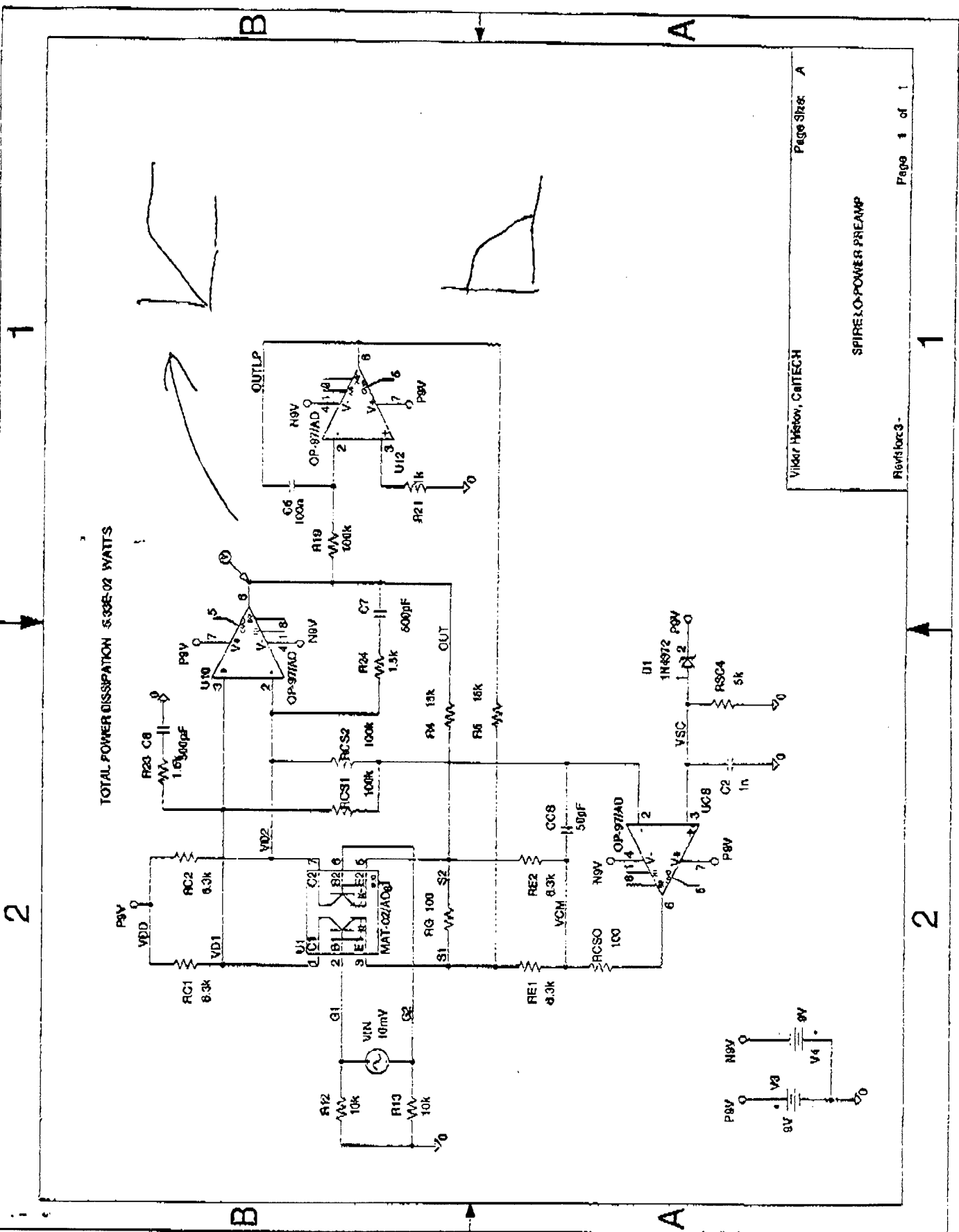
>
>Best Regards,

>
>Jamie

>
>+++++

>James J. Bock - Research Scientist Visiting Faculty
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>



Viktor Hserov, CATECH Page Sheet A

SPIRELO-POWER PREAMP

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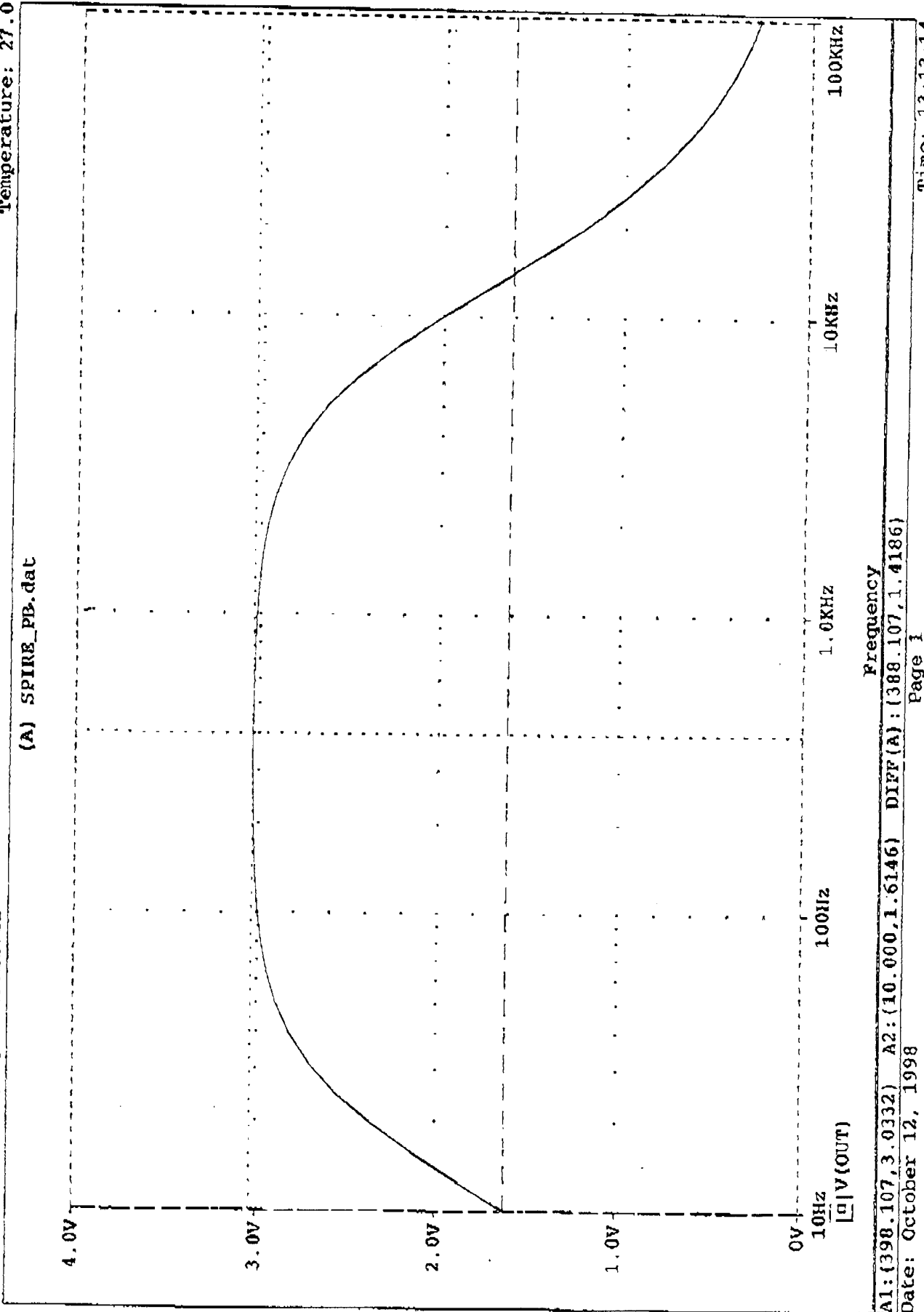
Rev:loc3-

* D:\MSim_8\Projects\SPIRE_PA\SPIRE_PB.sch

Date/Time run: 10/12/98 13:12:42

Temperature: 27.0

(A) SPIRE_PB.dat



Frequency

A1:(398.107,3.0332) A2:(10.000,1.6146) DIFF(A):(388.107,1.4186)

Date: October 12, 1998

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Time: 13:13:14

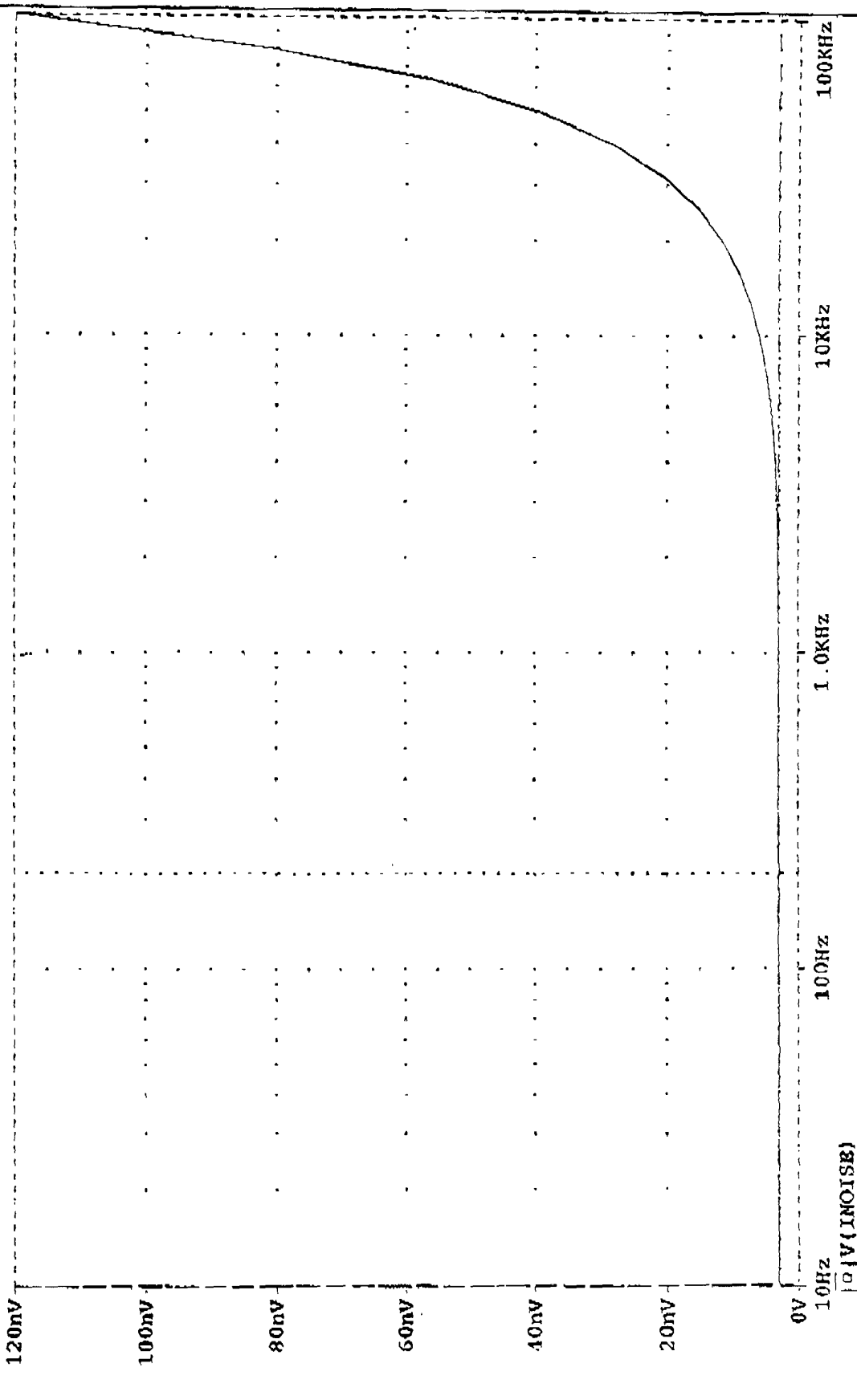
~~Gain~~ Gain vs. frequency

* D:\MSim_8\Projects\SPIRE_PA\SPIRE_PB.sch

Date/Time run: 10/12/98 13:12:42

Temperature: 27.0

(A) SPIRE_PB.dat



A1: (200.923 (2.9542n)) A2: (10.000, 3.0362n) DIFF(A): (190.923, -82.028p)

Date: October 12, 1998

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Time: 13:14:33

$V_n \sim 3nV/\sqrt{Hz}$



ADS7807
(A/D)

Low-Power 16-Bit Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

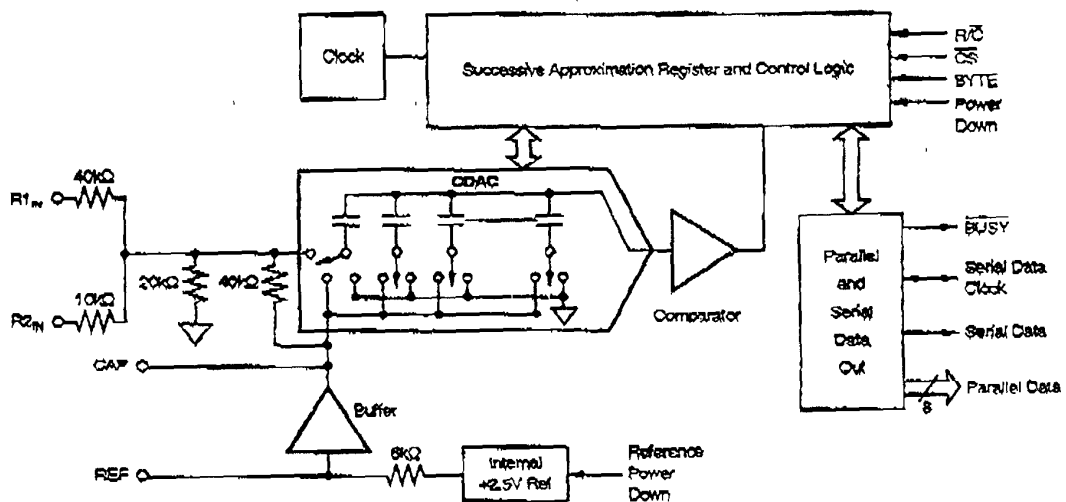
- 35mW max POWER DISSIPATION
- 50µW POWER DOWN MODE
- 25µs max ACQUISITION AND CONVERSION
- ±1.5LSB max INL
- DNL: 16 bits "No Missing Codes"
- 86dB min SINAD WITH 1kHz INPUT
- ±10V, 0V to +5V, AND 0V TO +4V INPUT RANGES
- SINGLE +5V SUPPLY OPERATION
- PARALLEL AND SERIAL DATA OUTPUT
- PIN-COMPATIBLE WITH 12-BIT ADS7806
- USES INTERNAL OR EXTERNAL REFERENCE
- 28-PIN 0.3" PLASTIC DIP AND SOIC

DESCRIPTION

The ADS7807 is a low-power, 16-bit, sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, clock, reference, and microprocessor interface with parallel and serial output drivers.

The ADS7807 can acquire and convert 16-bits to within ±1.5LSB in 25µs max while consuming only 35mW max. Laser-trimmed scaling resistors provide standard industrial input ranges of ±10V and 0V to +5V. In addition, a 0V to +4V range allows development of complete single supply systems.

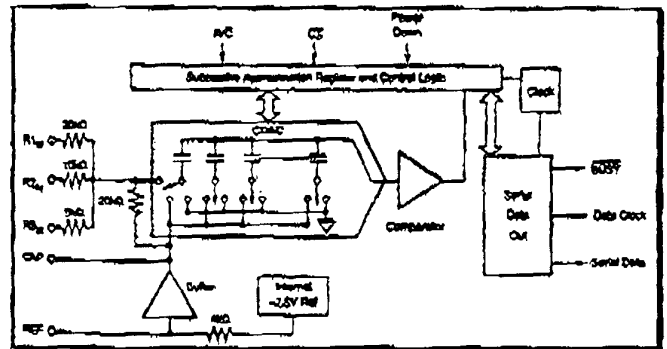
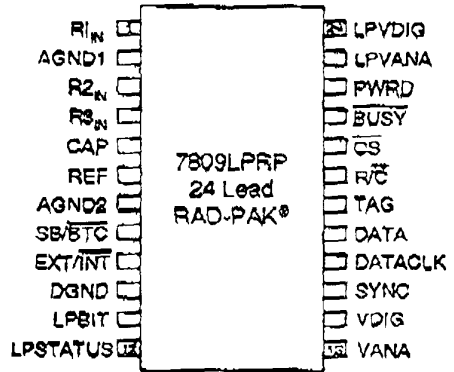
The 28-pin ADS7807 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial -40°C to +85°C temperature range.



International Airport Industrial Park • Billing Address: PO Box 11400 • Tucson, AZ 85714 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Tlx: 910-952-1111 • Cable: B&RCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SEi - Radiation Hardened 7809LPRP

16-bit Latchup Protected Analog-to-Digital Converter



Features:

- 16-Bit Organization
- RAD-PAK® Technology Hardened Against Natural Space Radiation
- Total Dose Hardness typ. 100 krad (Si)
- Latch-up Protection Technology (LPT™)
- Same Footprint as ADS7809
- Package: 24 Pin RAD-PAK® Flat Package
- 100 kHz min Sampling Rate
- ±10V and 0V to 5V Input Range
- Advanced CMOS Technology
- DNL: 16-Bits No Missing Codes⁷
- 86dB min SINAD with 45kHz Input
- Single +5V Supply Operation
- Utilizes Internal or External Reference
- Serial Output
- Power Dissipation: 132mW Max
- Screening per TM 5004
- QCI per TM5005

SEE 7809LPRP (RP for RAD-PAK®) high speed 16-bit analog to digital converter features a typical of 100 kilorad (Si) total dose tolerance. Using SEE's radiation hardened RAD-PAK® packaging technology, the 7809LPRP has the same footprint as ADS7809 and is latchup protected by Space Electronics Latchup Protection Technology (LPT™). It is a 24 pin, 16-bit sampling analog-to-digital converter using state-of-the-art CMOS structures. The 7809LPRP contains a 16-bit capacitor based SAR A/D with S/H, reference, clock, interface for microprocessor use, and serial output drivers. The 7809LPRP is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide various input ranges include ±10V and 0 to 5V, while the innovative design allows operation from a single +5V supply, with power dissipation of under 132mW. Capable of surviving space environments, the 7809LPRP is ideal for satellite, spacecraft, and space probe missions. The patented radiation hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing lifetime in orbit. This product is available in Class S packaging and screening.

Specifications and design are subject to change without notice.



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