SPIRE-JPL-NOT-000116-10

To: Matt Griffin November 19, 1998

Fr: Jamie Bock, Terry Cafferty, Dustin Crumb

Subject: Preliminary Thermal Design Summary for the SPIRE JFET Box

Dear Matt,

This memo summarizes our current consideration relative to the JFET box design. We have tried to simplify the matter so that it doesn't become overwhelmingly complicated. This memorandum is actually written for you and your team; we leave it to you to decide what and how best to present information contained herein to interested others.

INTRODUCTION

The backup option for the SPIRE focal plane arrays consists of ~150 detectors coupled to concentrating optics. The option requires 64 pointings to achieve a Nyquist-sampled map at 3 wavelength bands simultaneously. The detectors in the backup option consist of AC-biased NTD Ge spider-web bolometers with a cooled Si JFET readout placed as close to the detectors as possible (the '15 K' shield) to reduce the length of high impedance cabling.

The design of the JFET readout has now progressed to the point where the dissipated power per detector at the 15 K shield can be significantly reduced. The power dissipated per detector on all cryogenic stages can be reduced with a judicious choice of existing cabling used for SIRTF. Properly packaged connectors make operation of a large number of detectors tractable. We describe at some length designs of the JFET box, cabling, and connectors in the hopes that we can better understand their impact on the cryogenic system.

The scientific impact of increasing the number of detectors is significant, and the requirements on the observing modes are simplified. For example, with 600 detectors the time to map a region of sky to a limiting flux level is reduced by 2, and requires only 16 pointings. Attractive options also exist for intermediate numbers of detectors. For example, a mapping speed advantage of 2 can be achieved with 300 detectors by doubling the focal plane area and observing in a slow-scan mode. For an increase of detectors to 250, we could obtain a fully sampled map in 16 pointings by increasing the detector density in the 350 and 500μm channels, obtaining a mapping speed advantage at 350 and 500 μm of 1.6 and 2 relative to the backup option.

We present a design to readout 600 detectors with a Si JFET amplifier box based on Siliconix U401 dual Si JFETs thermally isolated on a lithographed membrane of silicon nitride. The JFET box resides on the '15 K' thermal shield, and the individual JFETs operate at a temperature of ~120 K. This design is based on experience with U401 JFETs used in a long-duration balloon-borne instrument, and careful measurements of the thermal and mechanical properties of silicon nitride membranes. The design is currently limited by the electrical power dissipated in the JFETs and source resistors. Further reduction in the dissipated power may be realized with lower-power JFETs and/or by moving the source resistors to a higher temperature stage. Given the significant scientific benefits, we request careful consideration of the tradeoff between power dissipation at 15 K and cabling resources with the benefits of increased mapping speed and simplified observing modes.

BASIC DESIGN APPROACH

The general approach is to mount the JFETs and their load resistors on silicon nitride membranes. The membrane acts as a structural support and a thermal isolator, as well as a substrate for electrical

connections to the JFETs. When the JFETs are powered, they self-warm to an operating temperature of ~120 K, and a temperature gradient is set up in the membrane. The outer edge of the membrane is thermally shorted to the '15K' level of the dewar. In addition to this basic configuration, we have the option of depositing a metallic thermal shunt strip on the membrane to bleed off heat and deliver it to a warmer temperature level within the dewar thermal shield system. However, this thermal shunt requires an interface to a higher temperature shield and does not reduce the average power dissipation.

We have limited our analyses to two configurations:

1. In the '15K only' case, the thermal shunt to the 30K dewar shield is eliminated, and the JFET box heat load is always entirely absorbed by the '15K' level of the dewar. In this case, the heat load from the JFET box into the '15K' level of the dewar is zero when the JFETs are not powered.

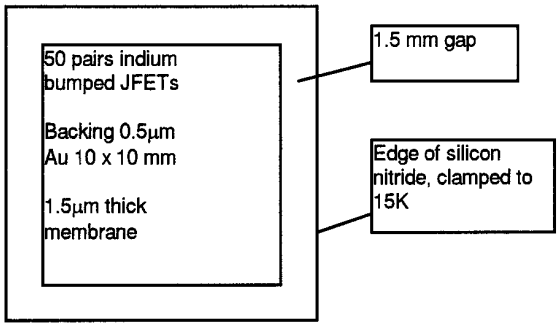


Figure 2: All heat delivered to 15K

2. In the '30K shunt' case, the bulk of the JFET heat load is shunted to the 30K dewar shield. In this case, there is a perpetual and essentially constant heat leak through the 30K shunt to the '15K ' level of the dewar. When the JFETs are not operating, the 30K shield 'gives back' (to the '15K' level) energy it absorbs while the JFETs are operational, so that the net energy absorbed by the 30K shield is reduced. This option significantly reduces the energy absorbed by the '15K' level, at the expense of an added thermal interface between the JFET box and the 30K dewar shield. A proposed membrane geometry (assuming 50 pairs of U401 JFETs dissipating 0.12 mW per pair packaged on each membrane) for this configuration is shown below:

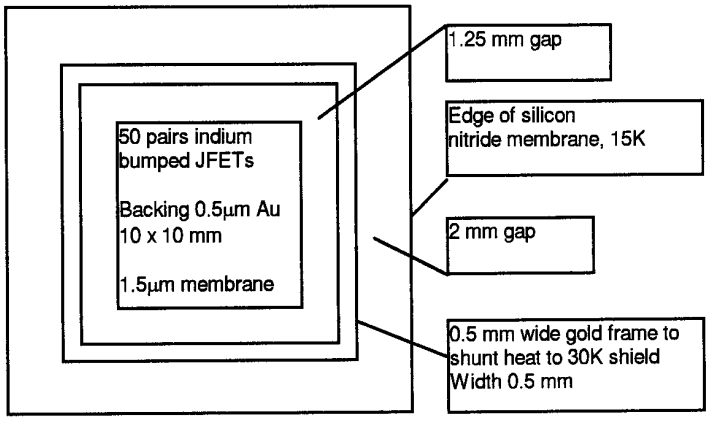


Figure 1: Membrane Geometry for '30K shunt'

The '30K shunt' option, while it has the advantage of reducing the heat load on the '15K' level of the dewar, has the general disadvantage that it is more complex. First, in order to bleed off the heat to the

30K shield, a thermal shunt consisting of a stranded copper wire with equivalent diameter (depending on length) on the order of 0.13-0.25 mm, must be attached to the gold shunt frame on the membrane. These wires (one for each membrane) pose a threat to the integrity of the membrane, and therefore must be secured (for purposes of relieving strain) to the '15K' frame to which the membrane is mounted. The strain relief mount is envisioned as a Vespel (polyimide) tubular post with length, outside and inside diameters respectively of 3, 1, and 0.6mm. One end of the post is bonded to the membrane frame, the other to the shunt wire.

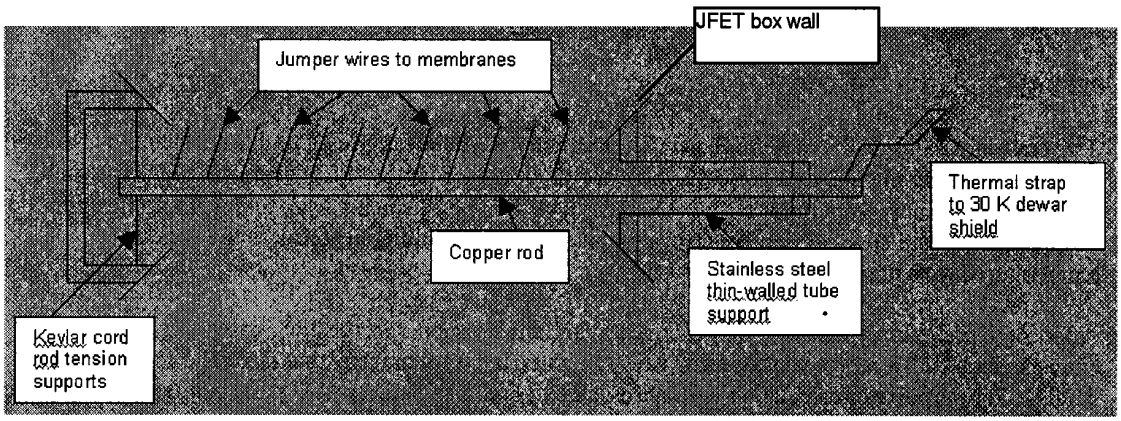
The other end of each wire is attached to a copper rod that penetrates (but is thermally isolated from) the JFET box. Thermal isolation of the rod from the JFET box is achieved using a combination of an RF-tight, thin-walled stainless steel tube at one end, and a Kevlar cord support at the other end, to allow for differential thermal contraction. This rod serves as a thermal bus making the conductive connections between the copper wires from all the membranes inside the JFET box, and to a flexible thermal strap to the 30K dewar shield outside the JFET box. (ESA currently makes no provision for such an interface, although they have indicated a willingness to entertain adding such a provision.)

Finally, the '30K' shield is predicted to operate at a temperature of approximately 130K during ground tests. Corresponding JFET operating temperature during ground tests would be on the order of 185K.

STRUCTURAL/THERMAL DESIGN DETAIL FOR THE '30 K SHUNT' CASE

For the 30 K shunt case, JFET heat from each membrane module (50 JFET pairs per module) is bled off through a 1-cm long stranded copper wire with copper cross-section equivalent to a solid wire with diameter 0.015 cm. This wire is strain relieved (to protect the membrane) by virtue of being bonded to a Vespel tube (3 mm length, 1 mm outside diameter, 0.5 mm inside diameter) at one end. The other end of the Vespel tube is bonded to the membrane frame at 15 K.

The shunt wire is then soldered to a copper rod that penetrates the JFET box wall (which is hard mounted to 15 K). This copper rod is supported at one end (7.6 cm outside the JFET box) by an RF-tight stainless steel tube of length 7.5 cm, outside diameter 0.5 cm and inside diameter 0.4 cm. The stainless steel tube is bonded to a shoulder on the copper rod (which clears the inside diameter of the stainless steel tube elsewhere by 0.05 cm). The 0.3 cm diameter solid copper rod traverses nearly the full length of the JFET box, and is positioned such that it comes in close proximity to all the membrane frames (which are stacked like cards) so that all the 30 K shunt wires can be attached to it conveniently. Its otherwise free end is secured radially by a Kevlar cord, to prevent radial motion while allowing axial thermal movement (due to differential thermal contraction) with respect to the copper rod, the JFET box and the stainless steel tube. This configuration is shown schematically below:



The heat leak associated with all 12 Vespel stand-offs is approximately 3.3 mW. The heat leak associated with the stainless steel support for the copper rod is approximately 2 mW. These parasitic heat leaks are accounted for in the models and included in the thermal analysis summary presented below.

SPIRE DUTY CYCLES

Regarding instrument duty cycle, we have assumed that SPIRE is 'on' 1/3 of the observation time; during this time, the other two instruments are 'off'. And when either of the other two instruments are 'on', SPIRE is 'off'. We have further assumed that the JFETs associated with the spectrometer are packaged together and separated from the modules containing the remainder of the JFETs, so that when the spectrometer is in use, the balance of JFETs activated during photometry dissipate no power. Spectrometry is assumed to use 1/6 of the total number of bolometers (and JFETs). We have treated three different duty cycles with respect to spectrometry and photometry: 100% spectrometry, 50/50, and 100% photometry. Other duty cycles can be derived from the two 100% duty cycles.

OTHER KEY ASSUMPTIONS

We select a membrane geometry that is optimized for all cases, to allow JFET self-heating to elevate the JFET temperature to ~120 K without the use of additional power. The thermal analyses reported in this memorandum are predicated on U401 JFETs (noise <~ $7nV/Hz^{-0.5}$ @ 100 Hz) operating near 120 K, and dissipating 0.12 mW per pair, including source resistors. We are also currently evaluating lower-power, lower-temperature JFETs from Goddard Space Flight Center (GSFC). We base our design on the U401 JFETs, noting that further improvement may be possible with GSFC JFETs.

ESA DEWAR HEAT LOAD SPECIFICATION

Our latest information regarding the 'acceptable' heat flow into the '15K' level of the dewar is (from Bernard Collaudin at ESTEC, in an email communication to me dated 20 August 1998) as follows: For each instrument (based on equal 1/3 duty cycles): 'ON' 14 mW; and 'OFF' 5 mW. From this, the corresponding allowable <u>average</u> heat flow to the '15K' level from each instrument is then 0.333(14) + 0.667(5) = 8 mW.

It is noteworthy that this specification is mute with respect to cable heat loads; perhaps this is a reflection of an assumption that the cable heat loads are small. While this may be an accurate assumption for instruments that multiplex before they come out, it is only true for SPIRE if the cables are designed for minimal heat leak. Therefore we present a detailed analysis of the heat load from the cryogenic cabling.

JFET CABLES TO THE CVV

Two leads are required for each JFET pair. A preliminary estimate of the allowable resistance per lead is 10KΩ. Assuming the 600-detector case, there are 1200 leads from the JFET box out to the dewar wall, and an equal number from the JFET box to colder levels. With this many leads and no multiplexing, cable materials and cross-section are critical importance to controlling heat leak to the various temperature levels in the dewar.

After some preliminary analysis, we generated a preliminary cable specification, based in part on conversations with a representative from Tayco Engineering, the company that made the cold cables for SIRTF. For purposes of calculation we have assumed 3-mil manganin twisted pairs bundled into stripline cables with an evaporated shield. The heat load is dominated by the thermal conduction of the manganin.

If heat load from the cables is an issue, Tayco can manufacture cables from finer wire, e.g. 1-mil or the 2-mil stainless instead of 3-mil manganin.

SPIRE Cryogenic Cable Specification (Proposed)

Temperature range of operation:	300 K to 2 K
Number of cables (JFETs to 2 K I/F)	12 ea + 3 ea spares = 15 total
Number of cables (JFETs to dewar wall)	12 ea + 3 ea spares = 15 total
Length (JFETs to 2 K I/F)	15 cm (6 in)
Length (JFETs to dewar wall)	1 m (40 in)
Conductors/cable	51
Conductor material	manganin
Conductor diameter	0.0075 cm (0.003 in)
Conductor spacing	0.002 cm centers (0.008 in)
Cover layers	0.005 cm (0.002 in) thick polyimide
Adhesive	0.0025 cm (0.001 in) thick Teflon
Shields (JFETs to 2 K I/F)	300 angstroms vapor-deposited Titanium
Shields (JFETs to dewar wall)	300 angstroms Titanium (plus 300 angstroms Au in warm section)
Connectors	Canon MDM 51-pin, Canon MDM 100-pin, Canon or Nanonics nanominiature

* Available from California fine wire at $135.00 per 1000 ft (~300 m)

The corresponding cable material cross-sectional areas are shown in the following table:

Material	Cross-sectional Area, cm^2
Manganin 3-mil (0.0075 cm) diameter	5.5 E-2
Kapton (polyimide)	0.31
Teflon (adhesive)	7.7E-2
Titanium	2.0E-4
Gold (warm section only)	2.0E-4

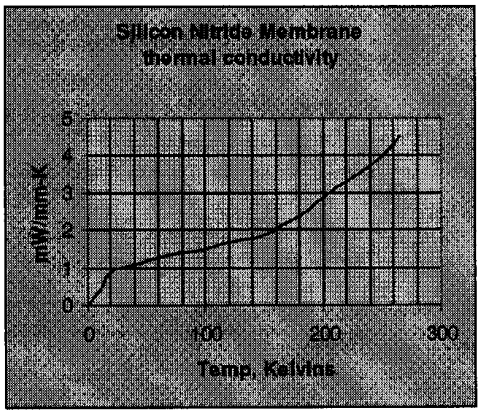
RADIATION EFFECTS

The membrane mounting technique for the U401 JFETs minimizes the 'hot' (~120 K) area to approximately 2 cm^2 for each module of 50 JFET pairs. Assuming this area radiates into a low-emittance (0.03) cavity, the total power radiated from the 12 modules is

$$12(2)cm^2(0.03)(\sigma)W\text{-}cm^{-2}\text{-}K^{-4}(114^4)K^4 = 0.7mW$$

MEMBRANE THERMAL CONDUCTIVITY

The thermal conductivity of one Si3N4 membrane has been measured as a function of temperature from 4K to near room temperature. This membrane had an outer square perimeter of 60mm and a 1mm gap between the outer perimeter and a gold-coated (0.5μ) central 'island', on which were mounted a heater and a temperature sensor. The thermal conductivity was derived from the membrane geometry and the power necessary to heat the island to a given temperature. The thermal conductivity as derived from these measurements is shown in the following plot. By placing two thermometers on the central gold island we determine that thermal non-uniformity of the island does not introduce more than 20 % error in the estimation of the thermal conductivity for T ≤ 120 K.



MEMBRANE ELECTRICAL TRACE CONDUCTION

Conductive heat transfer through the electrical traces deposited on the membrane (to connect the JFETs to the outside world) is negligible, as demonstrated by a recent thermal conductivity measurement. In this measurement (similar to that of the bare silicon nitride membrane measurement described above), the entire bare membrane was coated first with a 2 nm Ti / 15 nm Au layer.

The heater power required to heat the island to 120 K for the Ti/Au coated membrane was 1.35 times larger than that for the bare membrane, implying that the Ti/Au coating increased the conductance by a factor of 35 % relative to the bare membrane. Since the actual device will incorporate leads with a total width approximately 0.01 times the total width of the silicon nitride 'gap' (between 120 K and 15 K), the

conductance of the leads is inferred as (0.01)(1.35-1) = 0.0035 times the conductance due to the bare membrane. From this test we conclude that the conductance of the Ti/Au leads can be safely neglected.

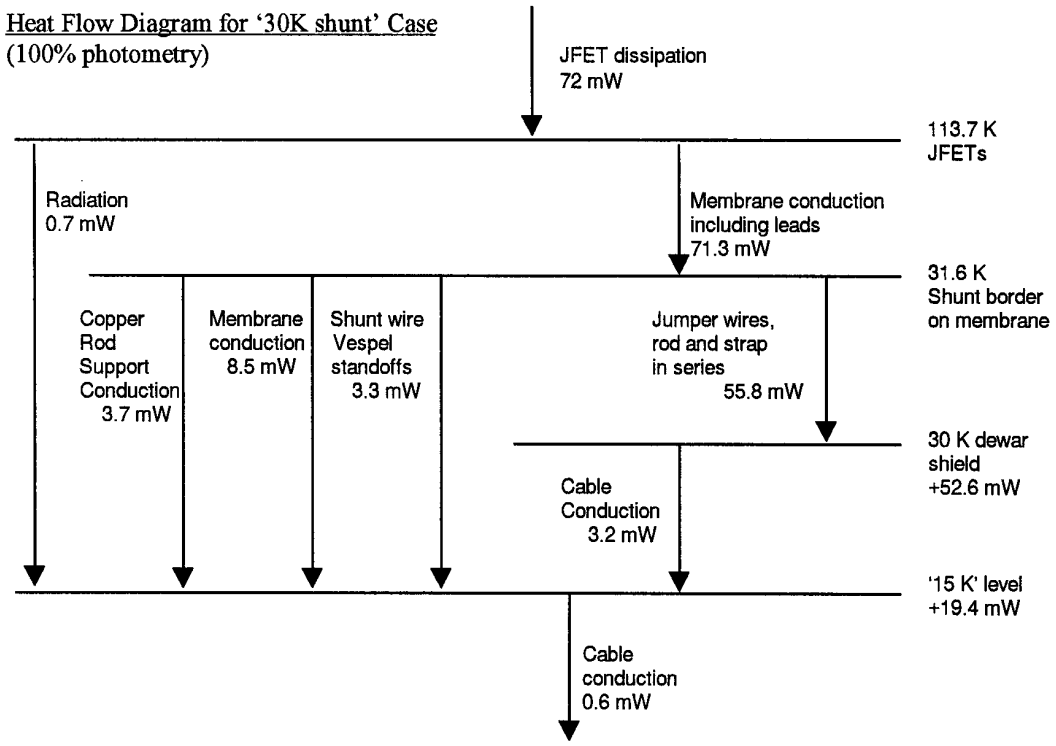
SUMMARY OF RESULTS

Thermal models of the two configurations described above were coded and solved using SINDA/G. Results for the two configurations are summarized in the following heat load tables and heat flow diagrams. The heat loads are representative of the 600 bolometer case. For a different spectrometry/photometry duty cycle, time weight the values for 100% spectrometry and photometry accordingly, and add them.

Table 1. Dewar Heat Loads from JFET Box for '30K Shunt' Configuration

SPIRE Mode	Peak Operational Heat Load		Average Heat Load*	
	To 30K dewar shield	To '15K' level	To 30K dewar shield	To '15K' level
100% Photometry	53 mW	19 mW	5 mW	19 mW
100% Spectrometry	-7 mW	17 mW	-14 mW	17 mW
50% Photometry and 50% Spectrometry	23 mW	18 mW	-5 mW	18 mW

* Based on 1/3 SPIRE operational duty cycle



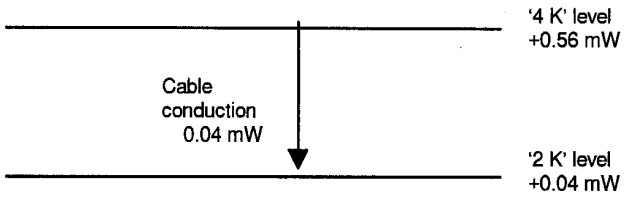
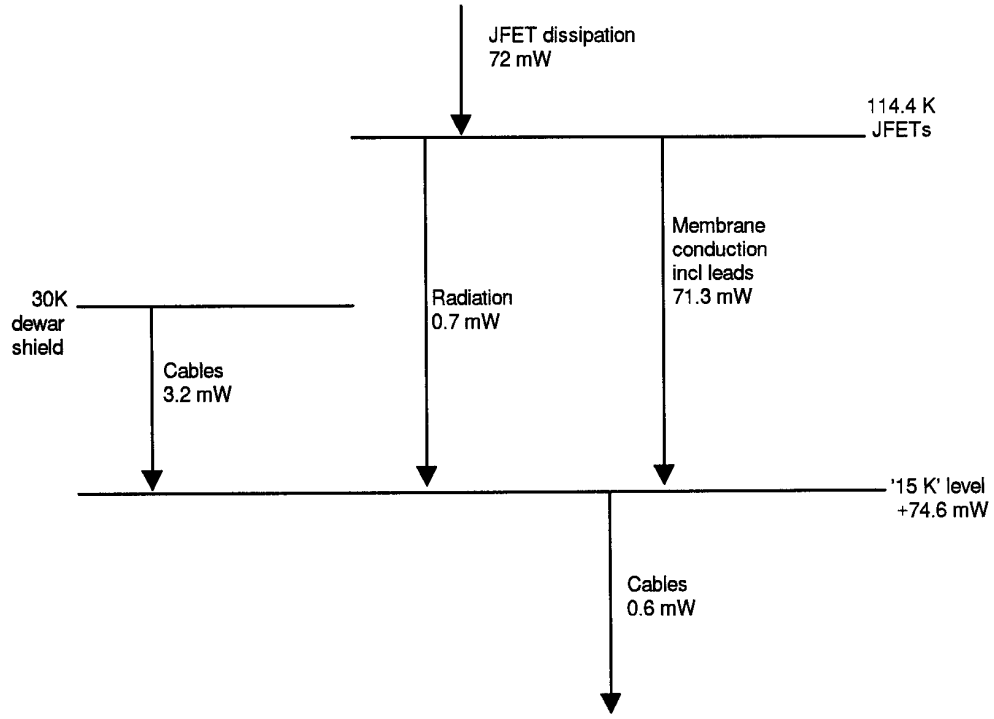


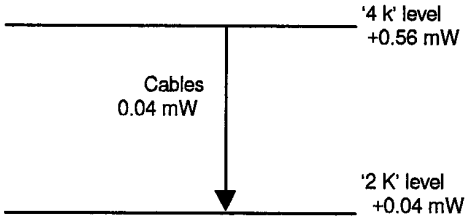
Table 2. Dewar '15K' Level Heat Loads from JFET Box for '15K Only' Configuration

SPIRE Mode	Peak Operational Heat Load (To '15K' level)	Average Heat Load* (To '15K' level)
100% Photometry	75 mW	27 mW
100% Spectrometry	15 mW	8 mW
50% Photometry and 50% Spectrometry	45 mW	17 mW

* Based on 1/3 SPIRE operational duty cycle

Heat Flow Diagram for '15 K only' Case
(100% photometry)





DISCUSSION

The '15 K only' option using 600 pairs of U401 JFETs exceeds the average ESA heat load specification for the 15 K level of the dewar by a factor of 2, assuming an equal photometry/spectrometry duty cycle. Assuming no improvement in the JFET performance, we would like to understand the implications for mission lifetime with this increased power dissipation.

The '30 K shunt' option has nominally equal average heat load onto the 15 K shield as the '15 K only' case, however, the peak power dissipation is lower. The average heat load on the higher temperature shield is small or even negative, depending on spectrometry/photometry duty cycle. Because the '30 K shunt' option requires a complex thermal interface to a higher temperature shield, and as the JFETs run at a considerably higher temperature in ground-based testing, we feel that the '15 K only' option is the superior choice if the peak power dissipation requirement on the 15 K shield can be relaxed.

FUTURE DEVELOPMENT:

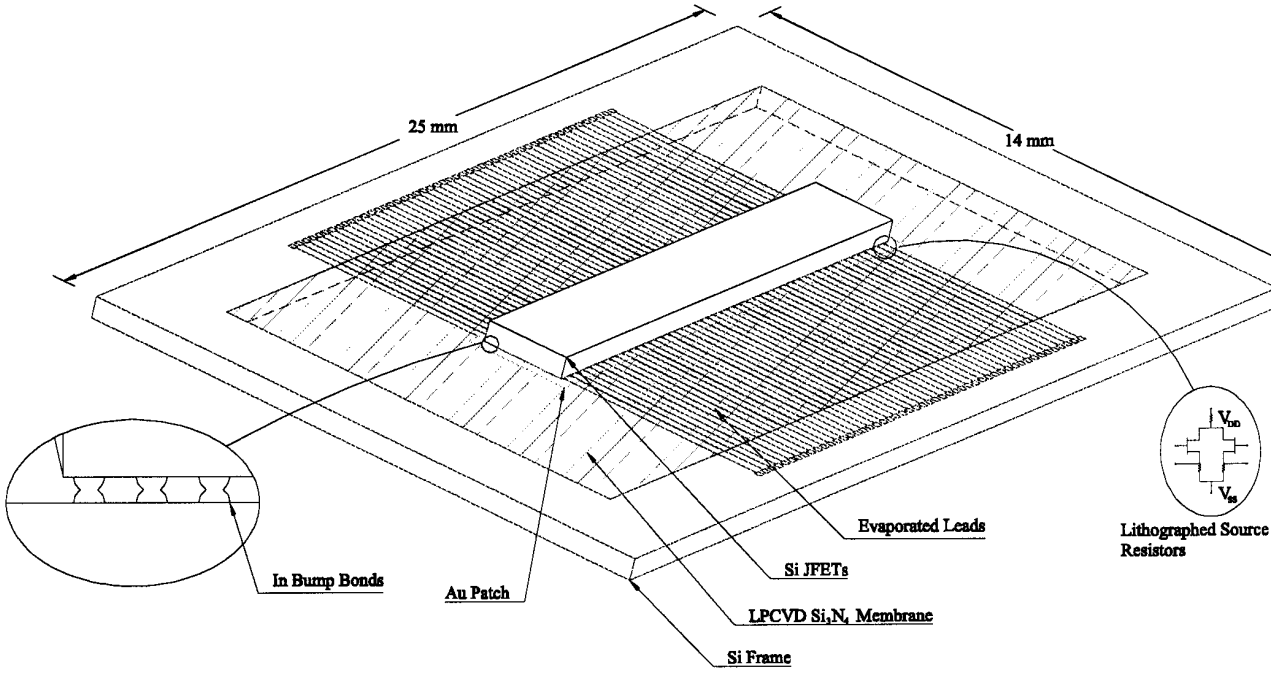
It is critical to the success of this JFET design option that the membranes be robust with respect to cold vibration and thermal cycling, and that they also demonstrate predictable and stable thermal characteristics. To date we have thermally cycled ~10 1.5 μm thick Si3N4 membranes without failure. We have also vibration tested a single membrane supporting a 30 mg test mass under a 40 g sine-sweep at room temperature, again without failure. We will undertake a program to systematically measure the thermal conduction, thermally cycle, and cryogenically vibration-test membranes that vary in composition and thickness.

We are currently investigating the possibility of manufacturing a monolithic die of matched JFETs pairs. Preliminary indications from GSFC and Siliconix are that the device yield, noise, and matching should be sufficient to allow regions of JFETs to be selected from a single wafer. The large die of JFETs will then be attached to the membrane (before the silicon is removed behind the membrane) by means of In bump-bonds. Individual JFETs may be mounted to the membrane and connected by means of wire bonds, but the assembly process is longer and the area per detector is larger. We will begin fabrication of a prototype using the In bump-bond hybridization technique.

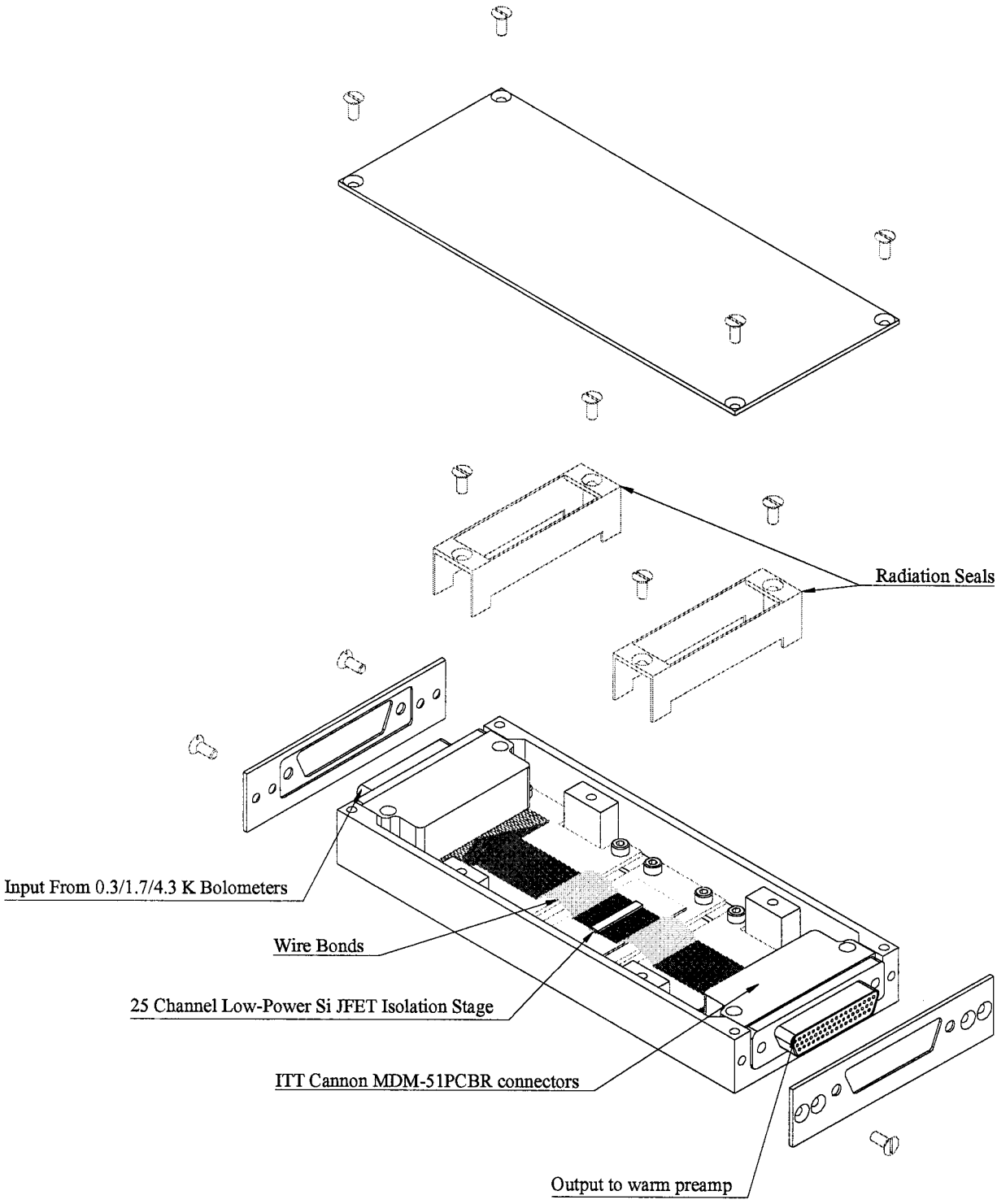
Low heat leak cabling is critical for increasing the format of the backup option. We can provide information as to the cost and space qualification of cables manufactured by Tayco. The bolocam cables currently use 3-mil manganin wire for ease of use.

Examination of the accompanying design drawings for the 600 JFET pair box will lead the reader quickly to the conclusion that connectors are dominant in setting the size of the JFET box. The drawings presented assume the use of Canon MDM 51-pin microminiature connectors. We understand that even these connectors are not currently approved for use by ESA. The authors know of numerous instruments using MDM 51-pin microminiature connectors for similar low-noise applications at cryogenic temperatures, and are unaware of even a single connector failure after years of use. Further reduction in

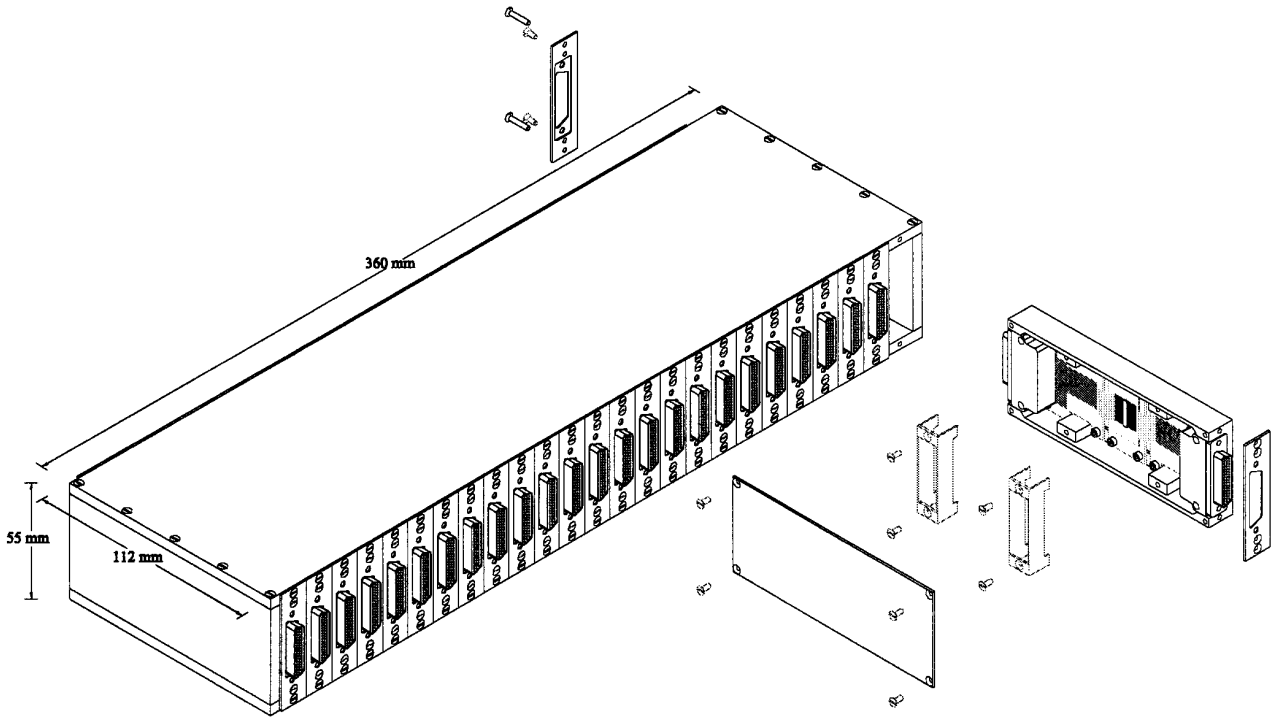
the volume and mass of the connectors may be obtained by use of connectors with larger format, e.g. ITT Canon MDM 100-pin, or higher density connectors, such as Nanonics connectors. We will evaluate candidate connectors for low-temperature, low-noise applications if ESA is open to their use in SPIRE.



Low-Power Si JFET Isolation Stage
25 Channel



25 Channel Low-Power Si JFET Module



Low-Power Si JFETs
Twenty Five, 25 Channel Modules