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From: "Ken King" <k.j.king@rl.ac.uk>
To: "Judy Long" <j.a.long@rl.ac.uk>
Subject: FW: Minutes of the SAp/IAC meeting held at IAC on Nov. 16, 1998
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-----Original Message-----
From: AUGUERES Jean-Louis DAPNIA [mailto:AUGUERES@DAPNIA.CEA.FR]
Sent: 24 November 1998 17:01
To: 'Griffin M.'; 'King Ken'; 'Swinyard Bruce'; 'Perez Ismael'
Cc: Bouère A.; Cara C.; Doumayrou E.; Le Pennec Y.; Loubère Françoise; Martignac J.; Rodriguez L.; Tourette T.; Vigroux L.
Subject: Minutes of the SAp/IAC meeting held at IAC on Nov. 16, 1998

Ref. numb.: SAp-SPIRE-JLA-0009-98
Action : for information
Date : 24-Nov-1998
Subject : Minutes of the SAp/IAC meeting held at IAC on Nov. 16, 1998
Author : J-L.Augueres, C.Cara, J.Herreros (IAC)
Dist.list : M.Griffin, K.King, B.Swinyard, L.Rodriguez, L.Vigroux I.Perez (IAC)
Cc : SPIRE SAp team
Ref :

Minutes of the SAp/IAC meeting held at IAC on November 16, 1998

Attendees: IAC: J.Herreros
SAp: J-L.Augueres, C.Cara

1. Meeting goals.

This meeting aimed at summing up the current situation regarding the SPIRE electronics and the works so far carried out as well as planned by IAC on SPU design.

It is to be considered as a kick off meeting to start the collaboration between IAC and SAp concerning both the managerial and technical aspects.

2. IAC situation.

IAC - stressed that IAC is involved in both LFI, SPIRE and PACS projects. For these three projects, IAC is committed to provide the Signal Processing Units (SPUs). On LFI, IAC is in charge to provide the DPU as well.

- the development of the SPUs on the three instruments rely on their potential commonalities.

- the funding has been granted by the Spanish Space agency on the basis of a first estimation. However, it is likely that any departure from the baseline could be a problem.

- the human resources from IAC is limited to 2 people. Most of the work will be carried out by the industry.

3. Managerial issues.

3.1 Overall SPIRE schedule.

SAp - presented the SPIRE high level schedule (both ESA schedule compatible and the proposed funding compatible).

- the SPIRE schedule has to be compared with those of the other instruments.

3.2 SPIRE management plan (reporting issue).

Discussions were based on the draft issue of the Management Plan circulated by K.King.

SAp - stressed that, given the SAp responsibility about the delivery of the entire SPIRE electronics (apart from the DPU which is an IFSI responsibility), a direct reporting line from IAC to SAp concerning the SPU development and technical issue should be considered.

IAC - stated that it was agreed at PI level that IAC, as a Co-I Institute, has to keep a direct reporting line.

SAp - put forward that this wish does not concern the Co-I reporting line but the managerial line regarding the technical issue. Other labs like the LAS (for the FTS control electronics) and the LETI (for the detector and cold electronics development) will report through the SAP as well.

Given the opposite positions on that subject it was agreed that the point has to be discussed with both the PI, the Co-PI, the PM and the electronics system responsible.

3.3 SPIRE electronics vs. SPU (and DPU) development plan.

IAC - presented the IAC workplan driven by LFI.

It is divided into 3 phases:

1. Prototype
2. Design / Development
3. Manufacturing

IAC planned to have a "bread board" prototype (SPU + DPU) available late 99 along with a S/C interface simulator (already available at CRISA providing that the S/C interface comply with the ESA standard). Evaluation s/w will be available as well.

The goal of this prototype is manifold:

- Validation & refinement of the s/w design.
- Low level s/w exercising.

SAp - stressed that an SPU development plan should be available as a draft soon as possible. This plan should show the development logic, the needed inputs (requirements) and take into account delays required by administrative issues (call for tender, contract setting up,...).

***ACTION on IAC / JH to draft an SPU development plan.

The SPU development plan shall take the SPIRE workplan constraints into account.

3.4 IAC deliveries to SAp (s/w development prototype, AVM CQM, FM, FS).

IAC - proposes as baseline to deliver:

- . BBM one for S/W and H/W development.
- . AVM for ESA to be used as the AVM and later as CQM
- . PFM to be used as flight model.
- . FS spare boards for LFI/PACS and SPIRE will be available (the number is tbd)

SAp - presented a block diagram showing the configuration needed for the AVM, CQM and FM model.

AVM: As far as we (SAp) understand no SPU is needed. In principle, only a DPU along with an instrument simulator (PC with emulated DPU - SPU interface) are needed.

CQM: According to the high level SPIRE electronics architecture, the SPU connected to a local test unit are necessary. However, this SPU could be a prototype (using commercial grade components).

As the s/w development should start quite early prototypes should be needed at SAp as early as late 2000. The number of prototypes needed is TBD but as a first guess 2 of them should be needed (one for h/w development, one for s/w development) plus a spare.

FM: Full qualified SPU.

FS: Situation unclear.

SAp - emphasised that up to 3 prototype models should be needed as early as late 2000. These models will be needed for: electronics elaboration, s/w development and test and spare.

The maintenance of the delivered models has to be considered as well.

3.5 FIRST / PLANCK Commonalities issues (participation to the commonality working groups).

Discussions were based the preparation document circulated by P.Estaria about the Nov. 11 Commonality Steering Group meeting (not transmitted to JH).

Participation of JH to the group #1, #2 and possibly #4 has to be considered.

Waiting for the outcomes of the Commonality Steering Group meeting (which took place on Nov. 11): new definition Of the groups are expected.

4. System issues.

4.1 SPU / DPU requirements.

SAp - SPIRE SPU requirements are not formally available yet. These requirements will be set up and discussed in the framework of the Electronics Working Group. At the last System meeting it has been agreed to address the question of the requirement on DPU and SPU as a whole before concentration on sharing between the two units.

IAC - presented the high level requirement document already available for LFI. DPU and SPU requirements are stated separately.

SAp - requirements (per model) shall be complete and classified:

. ICD reference (ESA document).
. functional h/w & s/w.
. mechanical.
. electrical.
. quality.
. packaging.
. ...

SPU requirements shall be reviewed at SPIRE level prior to

Concerning the memory requirement which is a concern, JH pointed out that the preliminary SPU system design already available does not limit the amount of memory which could be plugged as additional boards.

IAC - stressed that the cost of the memory chips is very high:

. $2000 for a Honeywell 128 kbytes chip.
. $1000 for a TEMIC equivalent.

The cost estimation made by IAC is based on 16 Mbytes of memory (see the above funding considerations).

SAp - pointed out that the amount of memory needed depends on factors not under control yet:

. detector technology.
. telemetry rate.
. onboard data reduction.

- It is not likely that the memory requirement could be stated before the detector technology choice and the PDR.

4.2 Overall SPIRE electronics architecture.

The SAp presented the overall electronics architecture.

Emphasis was put on the development philosophy consisting in having the possibility to run and test all the electronics independently from the DPU by the means of a local test unit interfaced to the SPU using the DPU interface.

Impact of the three concurrent detector options have been

discussed.

4.3 Mass and power budgets.

The estimation stated in the IIDB is based on the design presented and includes the DC/DC converters as well as cold redundancy.

4.4 Qualification program (thermic, vibration, EMI/EMC)

IAC - unit delivered will be qualified. Common qualification with PACS should be accepted by ESA.

Use of INTA facilities.

4.5 Components.

IAC - SMCS 332 (Scalable Multichannel Communication System) is qualified and available.

Integrated DSP from CRISA should be available by the end of this year.

Components should be chosen in the ESA list (pb. could arise with DC/DC converters but CRISA has the skill to design them). A careful check has to be carried out.

Standard components will be used for the Breadboard model as well as the AVM.

Military grade components could be used for the CQM.

4.6 Quality assurance.

IAC - is expecting that the quality assurance tasks will be carried out by the contractors as IAC has no resource nor particular expertise on Quality assurance.

No special care has been expressed so far on LFI (except LABEN) and PACS.

SAp - is regarding this issue as critical.

SAp - stressed that quality assurance requirements (e.g. production of a dedicated product assurance plan) have to be stated and quality assurance issues have to be monitored all along the development.

IAC - Support from SAp could be needed.

SAp - pointed out that, as the PA as to be involved at early Stage, the problem will be raised at the System Team level.

4.7 H/W vs. S/W sharing.

Not explicitly addressed.

4.8 SPU architecture and redundancies.

SAp - stress that the SPU proposed architecture has to be reviewed at system level.

Some remarks:

. apparent lack of watchdog.
. FIFO vs. Direct Memory acces (the serial communication link has to be assessed in term of efficiency and s/w programming impact).
. TSC21020 no more available in a standard grade.
. The efficiency vs. complexity and reliability of having two processors working in parallel has to be assessed. A priory the computing power gain could be as low as 1.5. It should be of a poor impact given the uncertainty bearing on the needed computing power. In addition it will increase the complexity and the cost while decreasing the reliability of the system.
. s/w downloading issue is unclear.

Redundancy on communication h/w is being studied in the LFI framework.

4.9 Test equipment (who is doing what)

Elaborating the DPU-SPU interface require a test unit.

Commonalities with the SPIRE local test unit: PC + interface boards + s/w drivers and communication layer.

Availability of a 4 link PCI board (+ drivers + training courses) from EONIC.

4.10 Harnesses.

IAC - not an IAC business.

The "warm" harness between the various "warm" instrument units will be delivered by the instrument teams, ...
(IID-A, 5.10.2.2, chap-page 5-29)

SAp - No explicit mention in the SPIRE management plan draft (3.2). It is not clear for the SPIRE 3 to SPIRE 2 harness.

- Test harnesses are likely of the responsibility of the SPIRE Consortium as well. In principle, it should be considered as part of the test units (or simulators) (TBC).

4.11 Deliverable documentation.

IAC - It will be provided by the industry.

4.12 Testing requirements and acceptance.

IAC - acceptances are made on the basis of the qualification test results as well as the documentation.

SAp - functional tests have to be performed as well.

4.13 Grounding & bounding scheme.

IAC - presented the LFI grounding scheme.

5. Software issues.

5.1 Development tools.

IAC - development tools are already available from Analog Device.

5.2 Real-time OS.

IAC - should be either VIRTUOSO or a customised R/T kernel developed by the industry (evaluation to be carried out on the Breadboard model).

SAp - A set of minimum requirements (to be stated) shall be met.

5.3 IAC / SAp S/W development: sharing, I/F.

Contribution of IAC to the s/w is limited to the low level communication drivers to be plugged in the VIRTUOSO R/T system and the validation s/w. JH thinks that most of the drivers could be commercially available.

6. H/W and technical issues.

6.1 DSP.

IAC - An ADSP 21020 (commercial equivalent for the TSC 21020) + SMCS chip without EDAC will be implemented on the Breadboard.

A TEMIC module including TSC 21020 + RAM + SMCS chip + Watchdog will be used for the further models.

6.2 SPU interfaces: with the DPU and with the DRCU.

IAC - an SMCS 332 chip is proposed. The maximum theoretical rate Is 200 Mbps via 3 links.

Presentation of a design for direct interfacing with h/w (ADC) i.e. which could be used for the DRCU. The DRCU acting as a slave of the SPU SMCS. In this case, one of the 3 links is used for the initialisation of the DRCU SMCS.

SAp - Full duplex communication shall be implemented (this allowing data and H/K to be transmitted via a single link).

6.3 DC/DC power supplies.

IAC - presented an overall scheme:

One single interface (s/c 28v (main + redundant)) is connected to a current limitation electronics (which responsibility is not clear yet (ESA, IFSI,...) this circuit fed independent DPU & SPU DC/DCs.

DC/DCs synchronisation to be decided (could be an ESA requirement).