From: MPEPL::OHB 23-JUN-1998 17:34:40.62 FIRST|ESA|M|004410
To: OHB ! SENT TO IN%"svolonte@hq.esa.fr"
CC:
Subj: For info: FIRST/Planck commonality meeting #2. Best regards, O.H. Bauer

Draft Agenda

FIRST/Planck Commonality Meeting #2

Date : July 8, 1998
Time : 09:00 - 17:00 LT
Place : ESTEC, Room Ca 327

Participants:

FIRST-PACS

Otto H. Bauer	MPE Garching
Erich Wiezorrek	MPE Garching

FIRST-HIFI

Henry Aarts	SRON Groningen
Douwe Beintema	SRON Groningen
Peter R. Roelfsema	SRON Groningen
Alain Cros	CESR Toulouse
Emmanuel Caux	CESR Toulouse

FIRST-SPIRE

Ken J. King	RAL
Jean-Louis Augueres	CEA Saclay

Planck-HFI

Richard Gispert	IAS Orsay
Jean-Luc Beney	LAL Orsay
Jaques Charra	IAS Orsay

Planck-LFI

Jose M. Herreros	IAC Tenerife
Renato Orfei	IFSI Rome
Riccardo Cerulli	IFSI Rome

FIRST/Planck Project

G"oran Pilbratt	ESTEC/AD
Peter Claes	ESTEC/AD
Pierre Estaria	ESTEC
Manfred von Hoegen	ESTEC
Ralf de Marino	ESTEC

Francis Vandenbussche ESTEC

Proposed Agenda
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(1) Adoption of the agenda

(2) Minutes of last meeting

(3) Commonality : How far can/should we push it?

(4) Digital electronics and on-board microprocessor(s)
- Status report — all teams
- Input from Project — M. von Hoegen/ R. de Marino

(5) Signal processing units
(On-board data reduction and compression)
- Status report — all teams

(6) Spacecraft interface simulator
- IFSI status report — R. Orfei
- Input from Project — F. Vandenbussche

(7) Instr. EGSE: RTA/QLA
- PACS concept — E. Wiezorrek/ O.H. Bauer
- Possible common development — all teams

(8) FINDAS
- FINDAS prototype status (VEGA) — P. Estaria
- Common ICC/DPC FINDAS interfaces — O.H. Bauer

(9) Other commonality aspects
- Project management (MS Project 98 ?), incl. Work Breakdown Structure
- Documents (MS Word, WordPerfect, Tex ?)
- Document management, incl. numbering system

(10) Schedules and Tiger Teams for different topics

(11) AOB

Comments are welcome!

Best regards and see you soon, Otto

Commonality Meeting # 2
8-Jul-98, ESTEC

Name	Institute	Instrument
Göran Pilbratt	ESA SCI-SA	FIRST project scientist
Alain CROS	CESR - TOULOUSE	HIFI -
Emmanuel CAUX	CESR - Toulouse - F	HIFI
Ken King	RAL - UK	SPIRE
Jacques CHARRA	IAS - ORSAY	HFI
Richard GISPERT	IAS - orsay - P	HPI
Jean-luc Bohey	LAL - ORSAY - F	HFI
JOSE MIGUEL HERREROS	IAC - Tenerife	LFI - PACS - SPIRE
RICCARDO CERULLI	IFSI - CNR	FIRST DPU
RENATO ORFEI	IFSI - CNR	FIRST - DPU
Erich Kreysrek	MPE - Garching	PACS
Michel Andrezyg	Estec, PL	
Ralf de Haan	ESTEC - TOS - QCT	
Manfred von Hoegen	Estec Field/Phase	PA Manager
PETER CLAES	Estec ESA SCI-SAF	FIRST - FINDAS SYSTEM ENGINEER
T. Passvogel	ESP/ESTEC	Projekt
Henri Aarts	SRON Utrecht	HIFI
Douwe Beintema	SRON Groningen	HIFI
Peter Roelfsema	SRON/Groningen	HIFI
J.L. AUGUÈRES	CEA	SPIRE
P. Estaria	ESA/ESTEC	Project
O.H. Bauer	MPE Garching	PACS

IFSI Status Report

Microprocessor:

TSC21020E Rad tolerant version of AD21020 DSP, best candidate because:

•Used in data compressor (our main interface) by Spanish colleagues in SPIRE and PACS.

•SW tools (C compilers debugger) and operating system (Eonic Virtuoso) available.

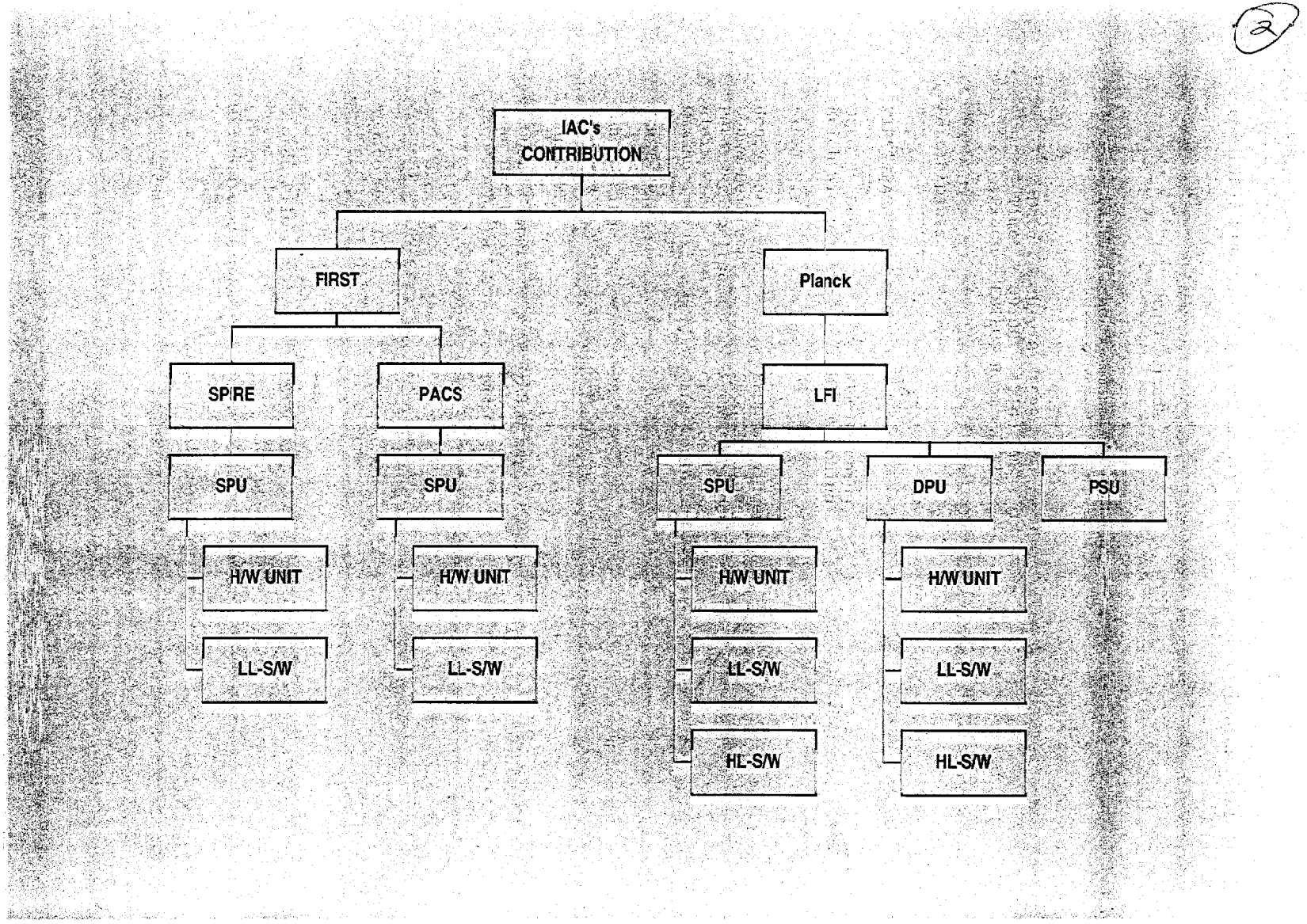
Information on possible microprocessors, requested to ESA and not received yet. We intend to participate to the ESA Common Components Procurement service, so we need ESA approval and/or suggestions on other chips.

Current actions:

Firm contacted on possible purchase of flight level computer boards based on TSC21020E. Offer received and under evaluation.

AD21020 DSP development kit purchased.

Preliminary planning defined.


IAC's CONTRIBUTION
FIRST
Planck
SPIRE
PACS
LFI
SPU
SPU
SPU
DPU
PSU
H/W UNIT
H/W UNIT
H/W UNIT
H/W UNIT
LL-S/W
LL-S/W
LL-S/W
LL-S/W
HL-S/W
HL-S/W

Common Aspects between the SPUs and the DPU

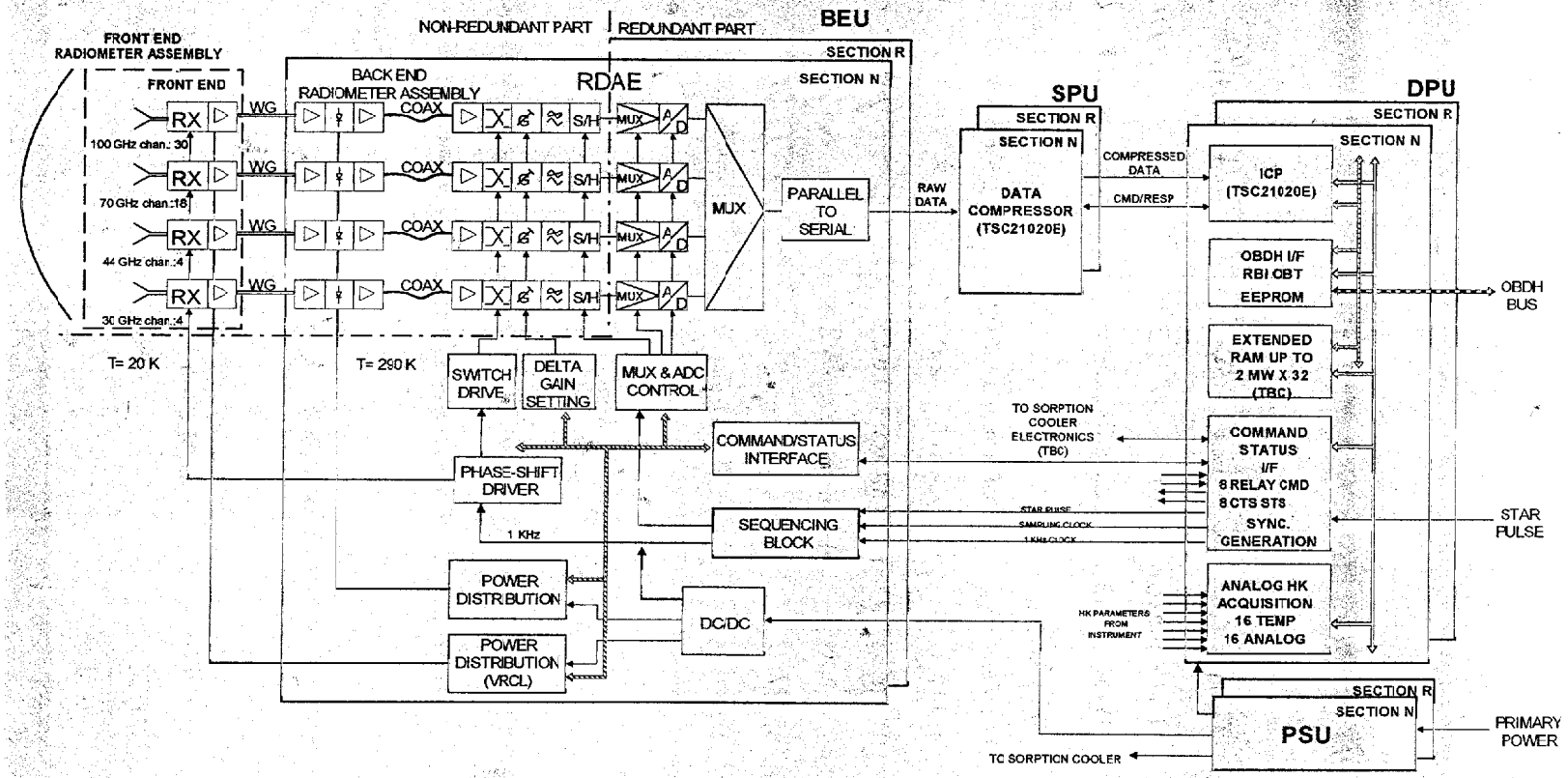
TSC21020E On-board microprocessor(s)

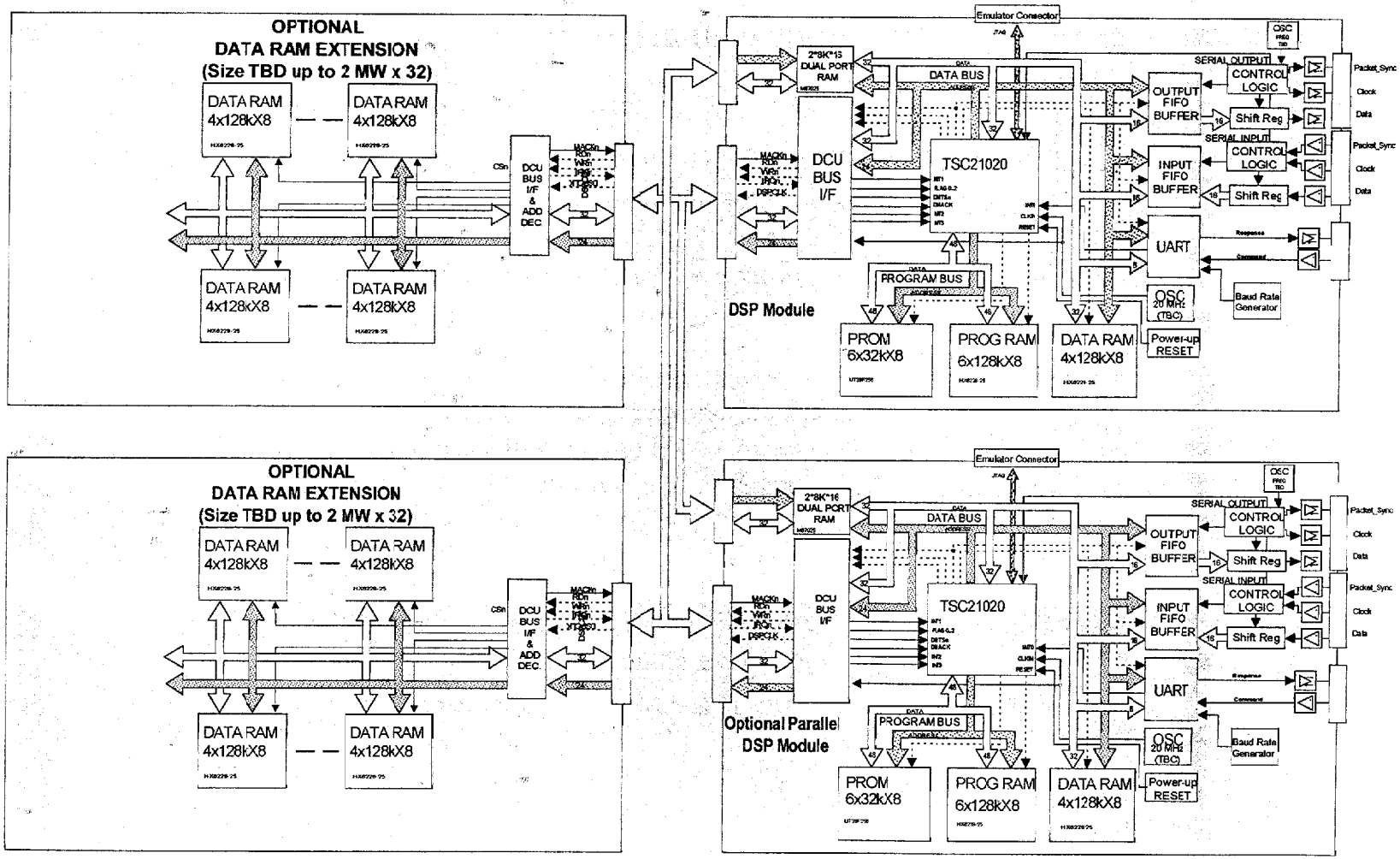
Development System

"C" On-board programming language

RS-422 Digital Serial I/F

2x Eurocard


FRONT END RADIOMETER ASSEMBLY
FRONT END
BACK END RADIOMETER ASSEMBLY
RDAE
NON-REDUNDANT PART
REDUNDANT PART
BEU
SECTION R
SECTION N
RX
WG
COAX
S/H
MUX
A/D
100 GHz chan.: 30
70 GHz chan.:18
44 GHz chan.:4
30 GHz chan.:4
T= 20 K
T= 290 K
SWITCH DRIVE
DELTA GAIN SETTING
MUX & ADC CONTROL
PARALLEL TO SERIAL
RAW DATA
COMMAND/STATUS INTERFACE
PHASE-SHIFT DRIVER
1 KHz
SEQUENCING BLOCK
POWER DISTRIBUTION
POWER DISTRIBUTION (VRCL)
DC/DC
SPU
DATA COMPRESSOR (TSC21020E)
COMPRESSED DATA
CMD/RESP
DPU
ICP (TSC21020E)
OBDH I/F RBI OBT EEPROM
OBDH BUS
EXTENDED RAM UP TO 2 MW X 32 (TBC)
TO SORPTION COOLER ELECTRONICS (TBC)
COMMAND STATUS I/F 8 RELAY CMD 8 CTS STS SYNC. GENERATION
STAR PULSE
SAMPLING CLOCK
1 KHz CLOCK
HK PARAMETERS FROM INSTRUMENT
ANALOG HK ACQUISITION 16 TEMP 16 ANALOG
PSU
PRIMARY POWER
TC SORPTION COOLER


OPTIONAL
DATA RAM EXTENSION
(Size TBD up to 2 MW x 32)
DATA RAM 4x128kX8
DATA RAM 4x128kX8
DATA RAM 4x128kX8
DATA RAM 4x128kX8
DCU BUS I/F & ADD DEC.
Emulator Connector
2*8K*16 DUAL PORT RAM
DATA BUS
DCU BUS I/F
TSC21020
PROGRAM BUS
DSP Module
PROM 6x32kX8
PROG RAM 6x128kX8
DATA RAM 4x128kX8
OUTPUT FIFO BUFFER
INPUT FIFO BUFFER
SERIAL OUTPUT
SERIAL INPUT
CONTROL LOGIC
Shift Reg
UART
OSC 20 MHz (TBC)
Power-up RESET
Baud Rate Generator
Packet_Sync
Clock
Data
OPTIONAL
DATA RAM EXTENSION
(Size TBD up to 2 MW x 32)
DATA RAM 4x128kX8
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Emulator Connector
2*8K*16 DUAL PORT RAM
DATA BUS
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TSC21020
PROGRAM BUS
Optional Parallel DSP Module
PROM 6x32kX8
PROG RAM 6x128kX8
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OUTPUT FIFO BUFFER
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SERIAL INPUT
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Shift Reg
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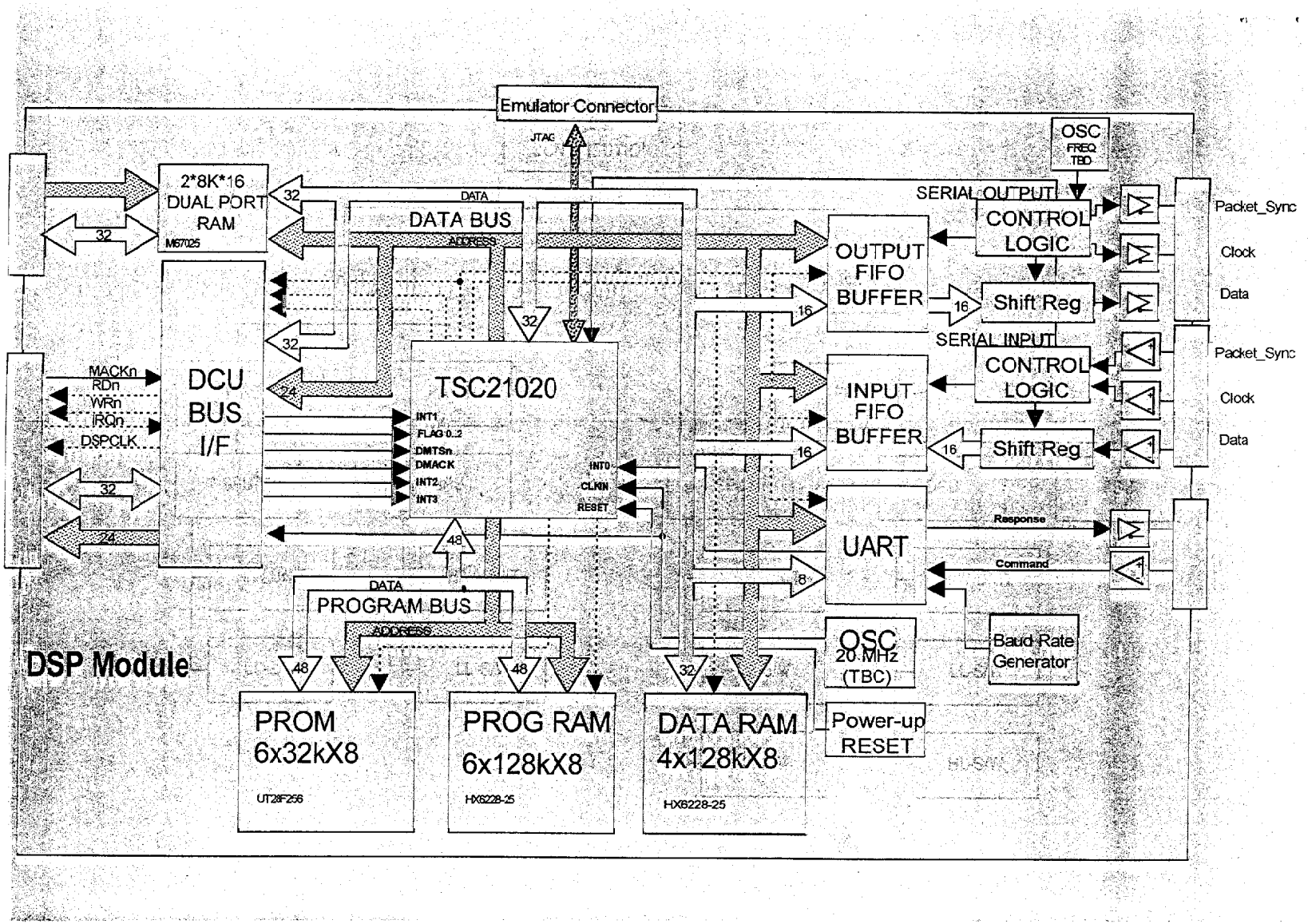
OSC 20 MHz (TBC)
Power-up RESET
Baud Rate Generator
Packet_Sync
Clock
Data


Emulator Connector
JTAG
2*8K*16
DUAL PORT
RAM
M67025
32
32
DATA
DATA BUS
ADDRESS
32
32
24
DCU
BUS
I/F
MACKn
RDn
WRn
IRQn
DSPCLK
32
24
TSC21020
INT1
FLAG 0..2
DMTSn
DMACK
INT2
INT3
INT0
CLKIN
RESET
48
DATA
PROGRAM BUS
ADDRESS
48
48
32
PROM
6x32kX8
UT28F256
PROG RAM
6x128kX8
HX6228-25
DATA RAM
4x128kX8
HX6228-25
DSP Module
OSC
FREQ
TBD
SERIAL OUTPUT
CONTROL
LOGIC
OUTPUT
FIFO
BUFFER
16
16
Shift Reg
SERIAL INPUT
CONTROL
LOGIC
INPUT
FIFO
BUFFER
16
16
Shift Reg
UART
8
Response
Command
OSC
20 MHz
(TBC)
Power-up
RESET
Baud Rate
Generator
Packet_Sync
Clock
Data
Packet_Sync
Clock
Data

DATA COMPRESSOR UNIT

The **Data Compressor Unit (DCU)** provides the hardware and software drivers needed to implement data compression algorithms in order to reduce the data rate of scientific data for the instruments of the FIRST/Planck satellite.

The core of the **Data Compressor Unit** is the Digital Signal Processor TSC21020E manufactured by MHS. This is a radiation tolerant version of the single-chip 32 bit floating point digital processor ADSP 21020 from Analog Devices.

This core provides, as basic functions, processing capability and serial interfaces (input and output). Optionally, the DCU, can provide RAM Extension modules (up to 2 MDWord 32 bits TBC), and a DC/DC converter. The DCU could include also, if needed, an additional DSP module working in parallel and communicated with the other via a dual port RAM.

The ADSP21020 is based on a external Harvard architecture. This means that provides two complete bus systems, one dedicated to program (instructions) and other dedicated to data. Concurrent access through both buses is possible, allowing simultaneous fetching and data, multiple data accessing, and parallel execution of arithmetic instructions.

These bus systems perform software programmable memory decoding, allowing to assign an individual memory range and memory cycle duration to each. The Program System Bus provides resources for two banks and the Data System Bus provides resources for four banks.

The Program System Bus is 48 bits wide and includes the PROM (32 KW TBC) memory bank and the program RAM bank (128 KW). The Data System Bus is 32 bits wide and includes the RAM bank for data (128 KW) and the memory locations used for internal and external DCU interfaces. One of these memory bank is reserved for the DCU internal bus.

The data processing throughput of this machine, running at 20 MHz (design baseline), is 75 MFLOPS peak and 50 MFLOPS as sustained performance. The instruction rate is 25 MIPS. Although this machine can carry out any type of control function (is in fact a general propose processor) it can execute the typical operations used in digital signal processor with a very high efficiency. The it can compute an 1024 points complex FFT in 780 us, a division in 240 ns, and an inverse of square root in 360 ns.

The DSP Module is controlled through a command/response (CRM I/F) asynchronous serial link (UART) from the DPU. This serial link is used to receive from the DPU commands, the own user software, implementing the compression algorithms, and patching of the DCU memory. The DCU transmit responses, containing status information, memory dumping etc. The protocol is based on a master/slave scheme, where the DPU is the master and the DCU the slave.

The DSP Module provides two simple unidirectional synchronous serial interfaces intended for receive scientific raw data and transmit compressed data. The DSP can access to these interfaces by means of FIFO buffers, that allow to decouple the execution of the software to the hard synchronism of the related serial lines.

External Electrical interfaces both serial links (raw data input and compressed data output) and the CRM I/F are based on the standard RS422.

Since the compression algorithm is not known, the baseline it to provide initially the processing throughput of the TSC21020E running at 20 MHz in order two allow the estimation of the margin when the processing load will be known. The same apply for the RAM and PROM sizes.

In the case that the processing throughput of the DSP is not enough to execute the foreseen compressing algorithm, it is possible to add an identical DSP Module working in parallel. The communication between processors is based on the use of a dual port RAM. This allows to implement cascaded sub-algorithms or parallelized algorithms. One of the DSP processors should act as data formatter and transmit the compressed data through its serial output.

Bootstrap code and software drivers to access to I/O devices are included in the provided PROM bank.

The bootstrap program will execute an initial self-test and then the user program will be charged from the DPU to RAM by means of the asynchronous serial line. After commanding from the DPU, the control will be left to the user program. It is also possible to provide basic on-flight support functions running in PROM, like specific self-tests programs or patch and dump of the user program in RAM from the asynchronous serial line, before execute it.

The development of the software drivers to access to the different devices of the DCU (input and output serial lines, interrupt service routines, asynchronous serial line...), by the responsible of the hardware development has the advantage of get a more efficient and simpler implementation, due to the better knowledge of the Hardware/Software interface.

The TSC21020E is supported with a complete set of software and hardware development tools from Analog Devices. It includes an in-circuit emulator supported through the JTAG port. This allow full-speed and non-intrusive access to the internal registers from a PC based development environment.

The available development tools are:

- Assembler
- Linker / Librarian
- Instruction level Simulator
- PROM Splitter
- C Compiler and Run Time Library
- C Source level Debugger, through the emulator
- Numerical C Compiler

Detailed description of the DSP module

The processor block is based on the TSC21020E IEEE floating-point Digital Signal Processor, that has separated program memory and data memory areas, accessed by independent address, data and control buses, following a Harvard architecture. The on-chip memory management along with the organisation of bus control signals allows

the definition of up to two program memory and up to four memory banks with programmable wait states and independent bank selects signals. Accesses can be programmed to be of up to seven wait states, with acknowledge, both or neither. Two independent data address generators provides full parallel access to data and instruction on single instruction.

Instructions forms a 48 bit orthogonal set supporting fully parallel data transfer and arithmetic operations in the same instruction.

Aside integer formats, it handles also 32 bit and 40 bit IEEE floating point formats. 32 bit precision is extended to 40 inside chip, limiting intermediate operation errors. This extended precision can be extended off-chip

Key features are:

- Architectural features directly support high-level programming language compilers
- Access to serial scan path (IEEE 1149.1 compatible) and on-chip emulation features.
- IEEE floating point formats
- Open memory system. Excepting a high-performance cache to avoid instruction fetching pipeline conflicts, no memory is located on-chip.
- On-chip memory management

The on-chip memory management allows the definitions of six independent memory areas. Each memory area can be programmed with different wait-state methods and numbers. Wait-states can be internally generated, externally with acknowledge, both or either, and the number of wait states can be extended from 0 to 7. This features are used in DSP MODULE reducing discrete logic and to define memory areas in which the different devices of the DCU are mapped.

Program memory bus consist of 24 bits address bus, 48 bits data bus and control signals /PMRD, /PMWR, /PMS0 and /PMS1.

Data memory bus consist of 32 bits address bus, 40 bits (32 as option) data bus and control signals /DMRD, /DMWR; /DMS0, /DMS1, /DMS2 and /DMS3.

The following banks or memory areas have been preliminary defined:

Accessed via program memory bus

Program memory ROM bank: from 00:0000 to 00:7FFF h (TBC)
Program memory RAM bank: from 80:0000 to 81:FFFF h (TBC)

and accessed via data memory bus:

Data Local RAM bank: from 0000:0000 to 0001:FFFF h (TBC)
FIFO and Local Dual Port RAM area: from 0002:0000 to 0002:FFFF h (TBC)
DSP MODULE I/O Port area: from 0003:0000 to 0003:000F h (TBC)

(Grouping serial interfaces and other registers located in the DSP MODULE)
Data Extension RAM bank: from 0004:0000 to FFFF:FFFF h (TBC), including Remote Dual port RAM

DSP MODULE I/O Port area uses the lower 4 bits (TBC) of Data Memory Address bus and control signals /DMDS3, /DMRD and /DMWR. The bank groups all registers and I/O Ports located in DSP MODULE, such control and data I/O Ports of CRM I/F, SERIAL OUTPUT I/F, Input FIFO and Output FIFO control registers and Watch-dog logic.

TSC21020E has four external interrupt lines, all of then maskeable. The assignation is TBD but it includes the synchronous serial lines, the dual port RAM and the UART.

Program memory ROM bank is organised in blocks of 6x32Kx8 (TBC) bits each, accessed as words of 48 bits or Triple Word (Twords). Initial Base line is total read-only memory space of 32KTword. Memory used is UT28F256 PROM. The use of bus control signals /PMS0 and /PMRD reduce the use of control logic to a minimum. PROM devices used have a 50 ns access time that will need of at least 1 wait state (with processor running at 20 MHz).

The final size of ROM bank is TBD depending of the user software.

Program memory RAM bank is organised in 1 block of 6x128Kx8 bits, accessed as words of 48 bits, or Tword, given a total program memory space of 128 KTword. Memory used is HX6228 RAM-SOI from Honeywell. The use of bus control signals /PMS1, /PMRD and /PMWR allows the use of no control logic to address this memory bank. The 25 ns access time allows operation with no wait states. (with processor running at 20 MHz).

Data memory RAM bank is organised in 1 block of 4x128Kx8 bits, accessed as words of 32 bits, or Double Words (Dword), given a total data memory space of 128 KDwords. Memory used is the same as in program memory RAM bank. As in this case, the use of data bus control signals /DMS0, /DMRD and /DMWR allows the use of no control logic to access this memory bank.

The **watch-dog** performs the user program sequence monitoring. The SW must access to watch-dog 8 bit register periodically to write the time-out value, a number between 0 and 255 to refresh it. When the counter reaches FFh a reset is raised to the processor. Since this counter is clocked by the processor clock divided by 8192, the timer has a programmable time-out of about 0,41 ms to 104.8 ms (TBC). If the user software lose the control, the watchdog output will trigger, and yield the processor to a known state.

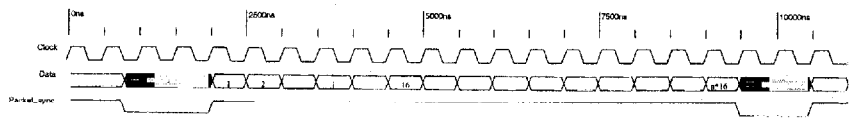
Both **synchronous serial links** share the same communication scheme, one as transmitter and the other as receiver. Electrical levels are RS422, and the signals are coded as NRZ-L.

Serial Clock frequency is based on a application dependent clock generator (TBD). Bit rates up to 5 MHz are possible (TBC).

The transmitter take data from the FIFO buffer, converts it to serial and put it on the line in synchronism with the rising edge of the clock. With the first bit (MSB), also with the rising edge, the Packet_sync signal goes high and remains in this state until the last bit has been transmitted, going to low with the rising edge after that. All three

signals are driven by the sender. The serial information transmitted are always an entire number of TBD bit words (may be 12 or 16).

The receiver samples the data line with the falling edge of the received clock from the instant in which the signal Packet_sync is sampled high until it goes low. It will feed a shift register with the serial data, count the pre-established number of bits, and store the parallel words in the input FIFO.



The messages should have a pre-established length (number of words) or a higher layer of the communication protocol (carried out by the software drivers TBC) should determine it from the content of the header of the message.

Serial Output I/F block is in charge of transmit scientific compressed data, and therefor it operates at low bit rates.

The FIFO buffer keep the DSP MODULE SW free of the synchronisation task when sending source data packets containing compressed scientific data. It is organised as an only write FIFO of 16Kx16 bits (TBC). The Output FIFO is read-out by Serial Output I/F control logic. Foreseen devices are 16Kx9 parallel FIFO M 672061 from MHS (smaller depths available).

After Serial Output I/F is enabled, the logic in this block will automatically start sending source packets whenever Output FIFO is not empty, reading data from it and sending through the synchronous Serial Output I/F. Logic distinguishes end of source packets when output FIFO is empty (TBC). Software driver must ensure that during a packet transmission output FIFO will not reach Empty condition until the transmission of the packet been sent finish.

Serial Input I/F is in charge of reception of measurement data samples, and therefor, it operates at high bit rates.

Input data are converted from serial to 16 bit parallel data and are filled in the input FIFO buffer. The DSP MODULE has only read access to this FIFO of 16Kx16 bits (TBC). The implementation is identical to the output FIFO. The flags of the FIFO (Empty, Half y Full) and the signal Packet_sync allow to implement the convenient access scheme to the FIFO by the software driver.

Access to FIFO area is made using the lower 16 bits of Data Memory Data bus, 1 address line of Data Memory Address bus, and Data Memory Control signals /DMS1, /DMRD and /DMWR. On-chip memory management features of processor allows an easy access control logic implementation. Due to access time use of 1 wait state is foreseen in this memory area.

The **CRM I/F** is based on 82C52 UART from HARRIS, implementing RS232 protocol with RS422 electrical levels. Baud rate is TBD.

All registers used to control and monitoring CRM I/F, as well as control and data I/O Ports of 82C52 are mapped and accessed via the DSP MODULE Port area memory bank. Registers addresses are TBD.

DSP MODULE can only access to its own RAM expansion bank. If two DSP Boards are present, each will have its independent expansion RAM bank. Communication between both processors takes place through Dual Port RAM based buffers, located in the expansion RAM bank address space.

Dual port RAM devices provide several synchronisation schemes (semaphores, flag registers with interrupt generation..) to allow consistent concurrent accesses.

The expansion memory bank uses 32 bit of Data Memory Data bus and Data Memory Control signals /DMS2, /DMRD and /DMWR. Use of /DMACK line is used to delay the memory cycle in case of conflict accessing to the dual port RAM

Preliminary DCU Budgets

This budgets are given with the hypothesis of one DSP module and one 2 MDWord RAM extension board in the DCU, implemented each in one Double Extended Eurocard board. Box dimensions and mass include all mechanical elements for the box. Power exclude the optional DC/DC converter or any power dissipated in power conditioning (regulation, protection, if needed)

Given numbers must be understood as a preliminary rough estimation.

Power Supply:	5 V DC
Power budget: DSP Module:	6 W
Expansion Memory Board:	1 W
Box Dimensions:	270 x 250 x 70
Mass:	3 Kg

EEE Parts Selection - Microprocessors 1

This is history now!

MAS 31750 family from GPS (UK)
(31750 µP, 31751 MMU, 31753 DMAC, ...)

If it can't be done without a MIL-STD-1750 microprocessor then there is still the PACE chipset from Performance Semiconductor (P1750A µP, P1753 MMU/COMBO, P1754 PIC) or the RISK based emulator chip from UTMC the UT1750AR

but on the following slides you will see what we rather recommend for new designs and applications

EEE Parts Selection - Microprocessors 2

SPARC V7 Chipset

- TSC691E IU, TSC692E FPU, TSC693E MEC
- MHS (F) on SCMOS1/2-RT (0.8µm CMOS)
- 10 MIPS, 2 MFLOPS @ 14 MHz, 2.2W @ 5V, 50 kRad(Si)
- wide range of SW development tools available
- used on DMS-R, COF, ERA, Microgravity Payload Computers

- CNES Evaluation starting Q3'98 - end '99
- ESA/SCC Comp. Detail Specifications available Q4'98
- Candidate for European PPL
- also proposed for eval. under NASA'98 comp. programme
- MCM version to be produced by MMS

EEE Parts Selection - Microprocessors 3

SPARC Outlook

- Single Chip Sparc V7 development kicked-off (Feb.'98)
- objective: chipset integration on SCMOS3-RTP (0.5µm CMOS), for pin-to-pin replacement in MEC position, 20 MHz, > 100 kRad(Si), <1.5W @ 5V, < 1 W @ 3V, first production parts planned to be available Q3'99

- pre-development studies for new generation SPARC V8
- possible development start mid 1999, expected availability 2002

EEE Parts Selection - Microprocessors 4

TSC21020E 32bit Floating Point Digital Signal Processor

- MHS (F) on SCMOS2-RT (0.6µm CMOS), 20 MIPS / 60 MFLOPS @ 20 MHz,
- 100 kRad(Si), SEU hard, Latch-up >100 MEV
- fully compatible with ADSP 21020 (comprehensively demonstrated during development),
- 256 pin MQFP, also available in PGA package for EM
- Rev. C prototype delivery cw28, final radiation tests cw34
- first procurement for METOP initiated (LAT 1)

- CNES evaluation planned: start in 2nd half of '98 to end '99
- ESA/SCC Component Detail Specification available Q4'98
- Candidate for European PPL
- Development of companion devices to be initiated

For details contact Ph. Armbruster TOS-ETD

EEE Parts Selection - Microprocessors 5

Other microprocessors (µP) / microcontrollers (µC) available:

- MC-80C32E 8bit µC from MHS (F), ESA/SCC 9521/002

- HS-80C85RH rad.hard 8bit µP from Harris (US), SMD 5962-95824
- HS-80C86RH rad.hard 16bit µP from Harris (US), SMD 5962-95722

- HS-RTX2010RH rad.hard 16bit RISC µC from Harris (US), SMD 5962-95635

Power PC

- TS-PC603e 32bit Microprocessor, 133MHz, from TCS (F), Motorola die, TS-PC603p 166MHz - 200MHz
  radiation testing to be performed by CNES
- other TS-68xxx family devices from TCS (F), Motorola die, available in QML Q level

EEE Parts Selection - Microprocessors 6

Procurement

- Lead times are subject to change
  => keep in touch with the manufacturer
  current range is 30 to 58 weeks

- Price Indication for
  40 parts or sets, ESA/SCC B, LAT 2 (20 test + 20 FM)
  SPARC = 19 kECU/set DSP = 7,8 kECU/part
  + LAT charges (min. buy for these types 5 parts/sets)

  EM prices: SPARC = 3,8 kECU DSP = 1,5 kECU

EEE Parts Selection - Information Sources

- The ESA/SCC Qualified Parts List is published bi-annualy in April and October
- The ESA PPL (ESA PSS-01-603, issue 3, 9/95) will be replaced by the
  European Preferred Parts List (ECSS-Q-60-xx)
  currently in preparation and planned for issue in Q4'98
- please consult: http://www.estec.esa.nl
  >ESTEC Technical Information >EEE Parts-ESA/SCC System
  for QPL and other useful ESA/SCC information

- The NASA Parts Selection List (NPSL) is replacing MIL-STD-975M and can be found at http://misspiggy.gsfc.nasa.gov/npsl
- The GSFC PPL can be found at http://arioch.gsfc.nasa.gov/ppl/ppl.html
- The MIL-QML/QPL is found at http://www.dscc.dla.mil/programs/qmlqpl/
- Radiation data can be obtained from http://flick.gsfc.nasa.gov/radhome.htm and http://radnet.jpl.nasa.gov

S/C Simulator

We need a number (3~4) of S/C simulators.

This is a standard piece of HW to be implemented with a PC board + software and eventually well documented.

We propose a common buy for all possible users:

- ESA should provide ASAP the I/F specifications.
- We should define the approximate N. of units.
- Setup a team to define (via E_mail) board specs.
- We propose ESA to ask for a quotation for N (~?) boards.
- We propose everybody to ask national firms for a quotation for N (~?) boards.

INTEGRAL Project Directory

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Software Manager	D. Burg		
Project Manager	B. Foltzer		
Hardware Manager	J.P. Horrgott		
Director	P. Künzli		

Ton van Overbeek 15.06.98 11:53

To: Harm Schaap/estec/ESA@ESA
cc:
Subject: ADELSY

Harm,

Here the detais:

ADELSY
Via Cantonale
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Tel. +41-91-8592851
Fax +41-91-8592852
Contact Person: Bruno Storni

Ton
P.S. ADELSY is in the ESTEC short-dial phone list

PROPOSED

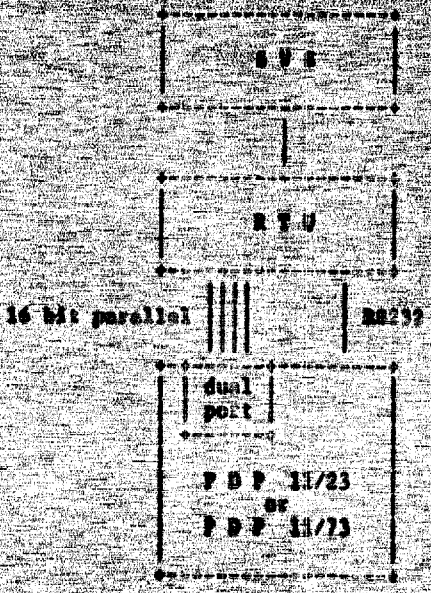
COMPUTER HARDWARE CONFIGURATIONS

FOR DIFFERENT CHECKOUT LEVELS

AND GROUND SEGMENT

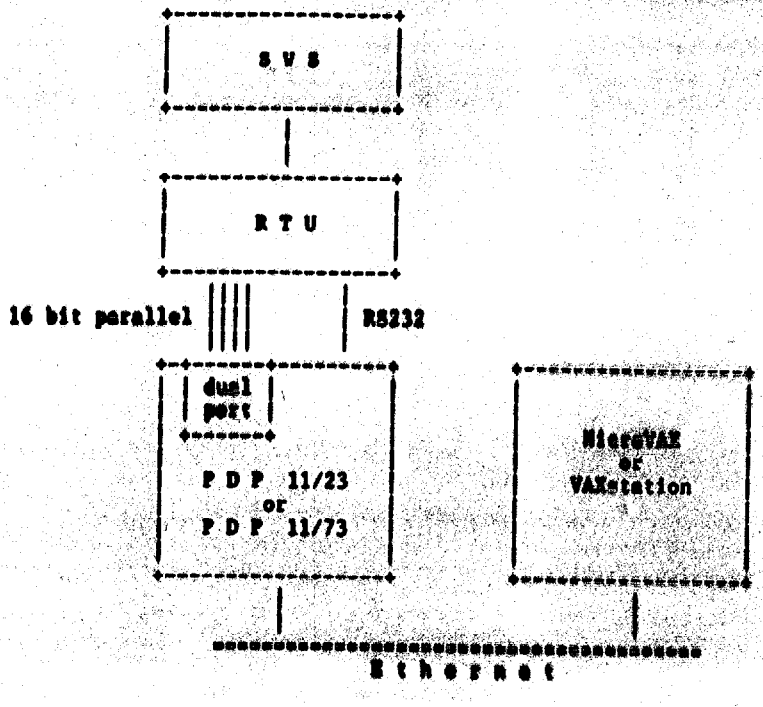
O.H. Bauer MPE-Garching

(1) Bench Level and Lower Instrument Level

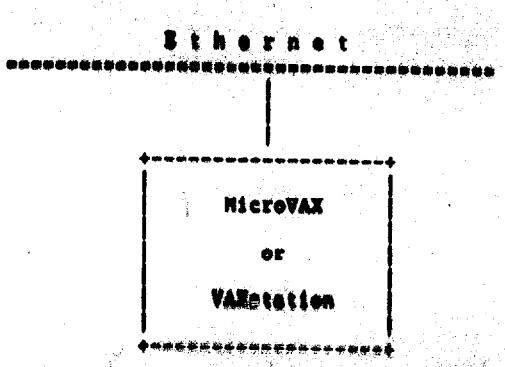


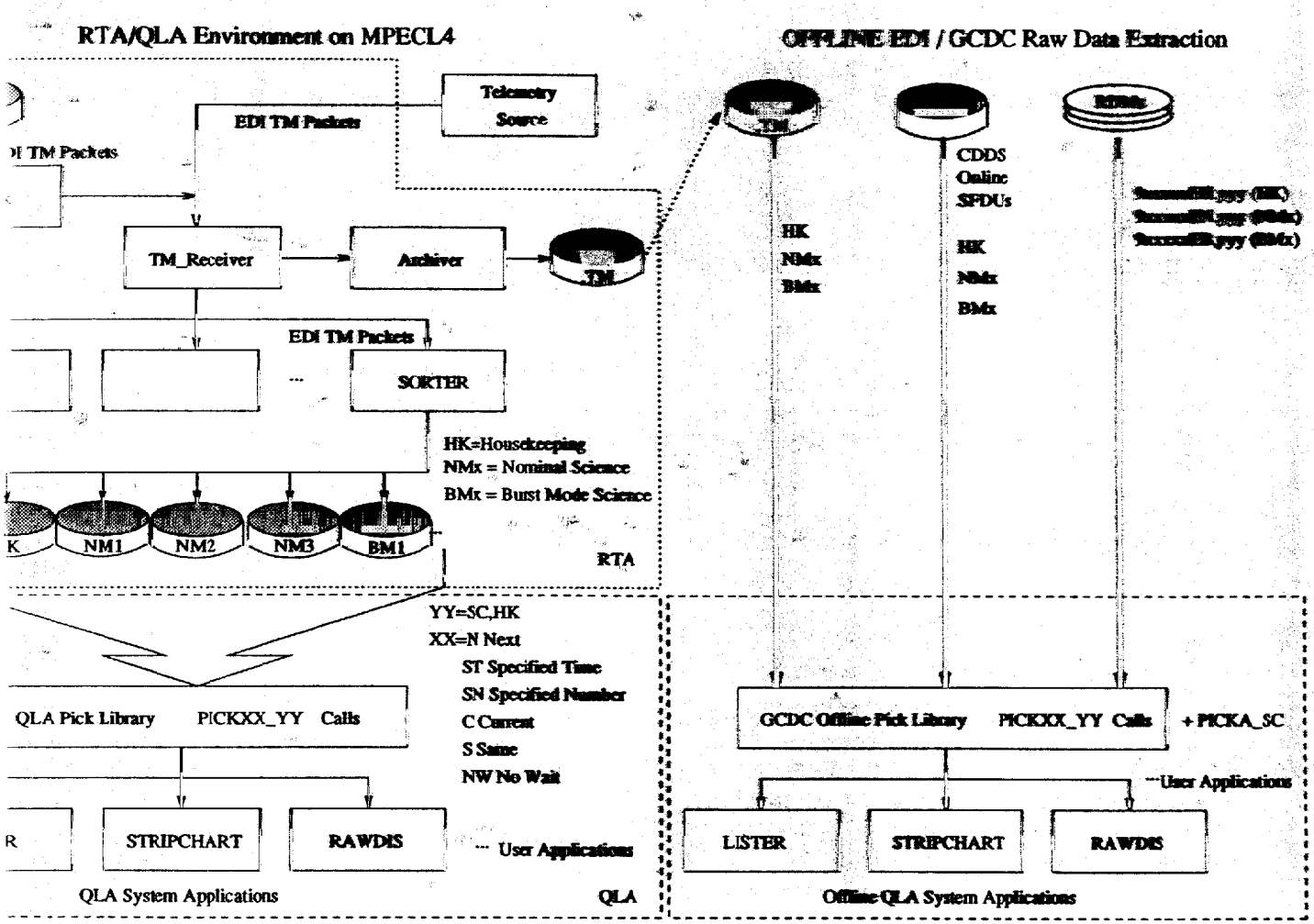
(2) Instrument Level

On Instrument Level the PDP 11/23(73) will be used as an intelligent interface for a MicroVAX or a VAXstation. The interface between the PDP and the VAX will be Ethernet.



(3) Sstem Level Tests and Ground Segment

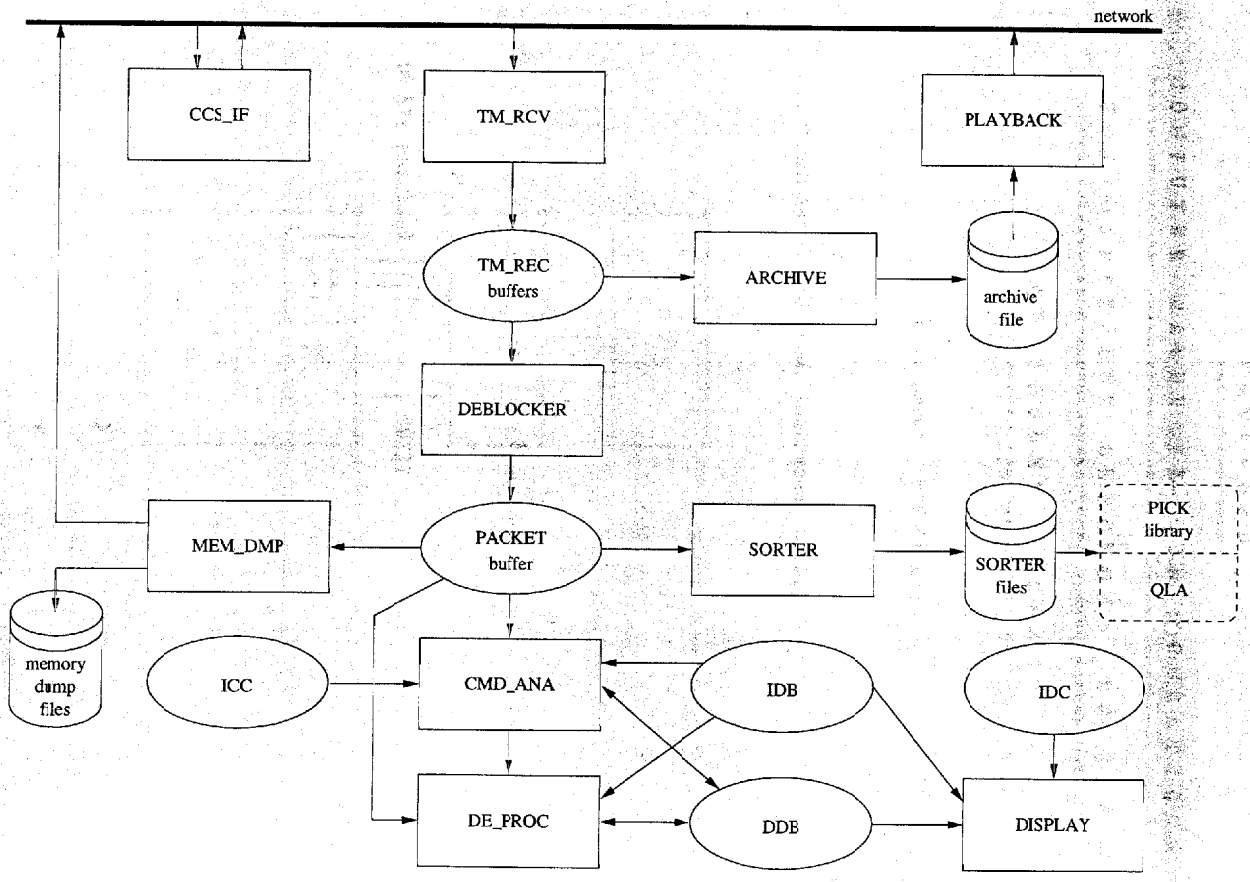



RTA/QLA Environment on MPECL4
OFFLINE EDI / GCDC Raw Data Extraction
Telemetry Source
EDI TM Packets
TM_Receiver
Archiver
TM
EDI TM Packets
SORTER
HK=Housekeeping
NMx = Nominal Science
BMx = Burst Mode Science
NM1
NM2
NM3
BM1
RTA
YY=SC,HK
XX=N Next
ST Specified Time
SN Specified Number
C Current
S Same
NW No Wait
QLA Pick Library PICKXX_YY Calls
STRIPCHART
RAWDIS
User Applications
QLA System Applications
QLA
HK
NMx
BMx
CDDS
Online
SFDUs
HK
NMx
BMx
GCDC Offline Pick Library PICKXX_YY Calls
+ PICKA_SC
User Applications
LISTER
STRIPCHART
RAWDIS
Offline QLA System Applications

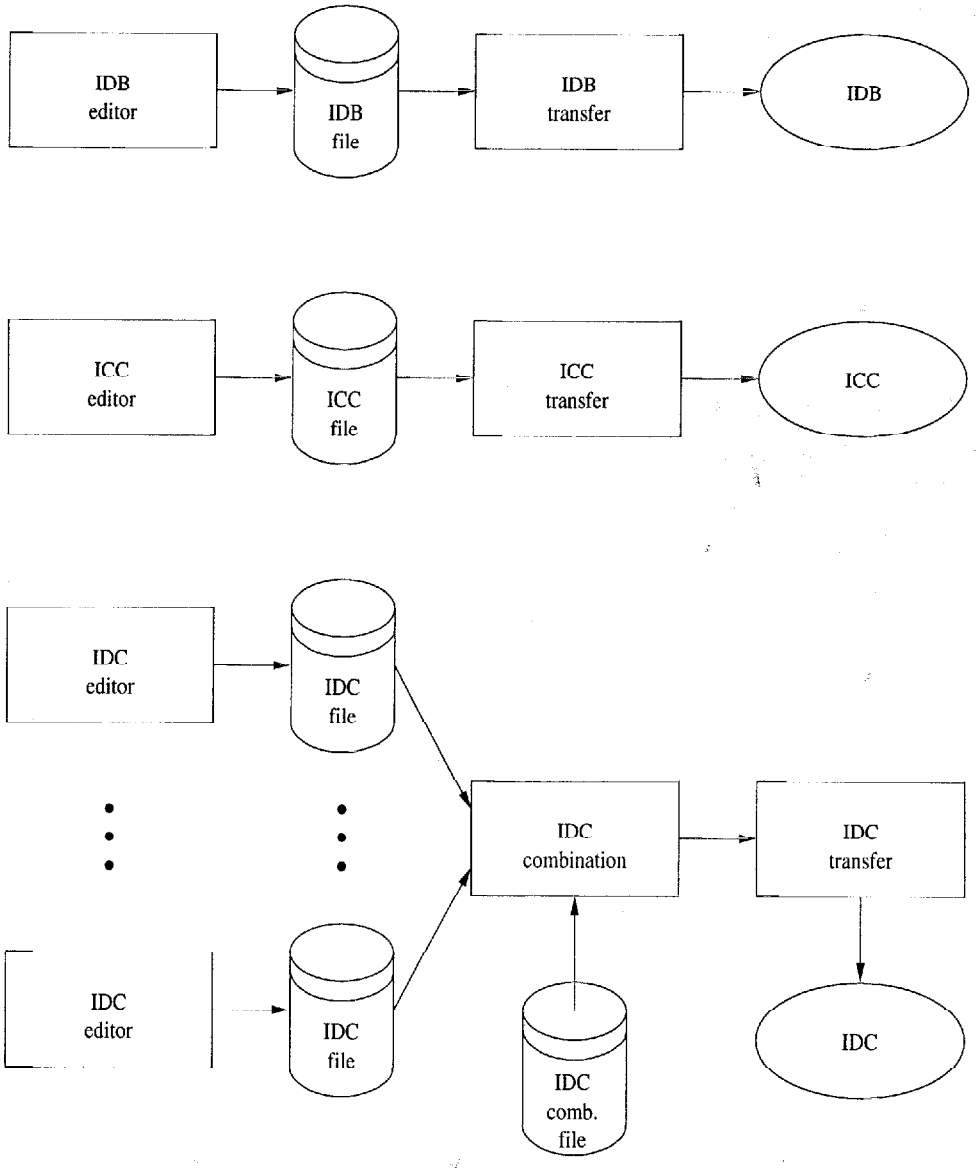
Major blocks in the online RTA diagram

TM_RCV	receives TM records over the network and stores them in the TM_REC buffers
TM_REC buffers	circular array of buffers to store TM records
ARCHIVE	copies the TM records to the archive file
DEBLOCKER	forms TM data packets by either breaking TM records into packets or assembling TM records into packets
PACKET buffer	buffer to store TM data packets
MEM_DMP	extracts memory dump information from TM data packets and write them to files or a remote server
SORTER	copies TM data packet to the SORTER files
SORTER files	the SORTER files are used together with the PICK library as QLA interface
CMD_ANA	extracts information about uplinked commands from the TM data packets, updates the DDB to reflect the new to be expected values for data entities (TM channels)
DE_PROC	extracts data entities (TM channels) from the TM data packets, converts them either to character strings (status parameters) or floating point values (analogue parameters), checks them against their limits and checks them against their commanded values
DISPLAY	displays the data entities using special screen layouts on a terminal device
IDB	Instrument DataBase: stores fixed information about data entities like how to extract and convert them, how to determine their limits ...
ICC	Instrument Command Characteristics base: stores fixed information about how to get the new commanded values for data entities from the uplinked commands
IDC	Instrument Display Characteristics base: stores fixed information about how to compose the different screen layouts for the DISPLAY pages
DDB	Dynamic DataBase: stores the actual (current) data for the data entities like raw value, converted value, actual limits ...

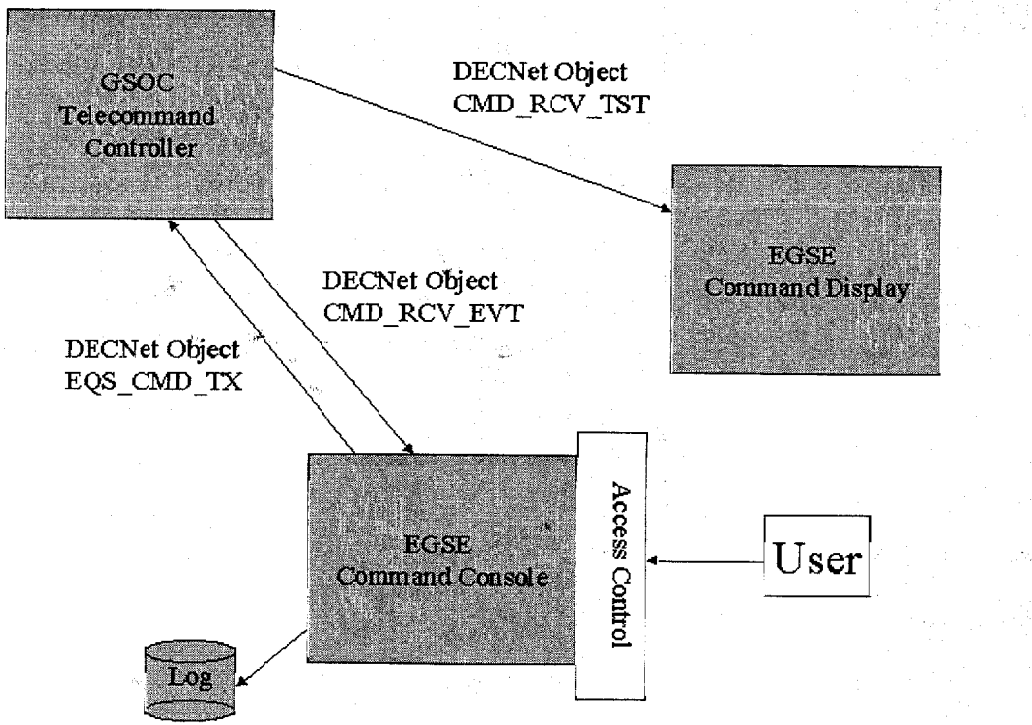
Online processes, files and commons of the current RTA



Offline processes, files and commons of the current RTA



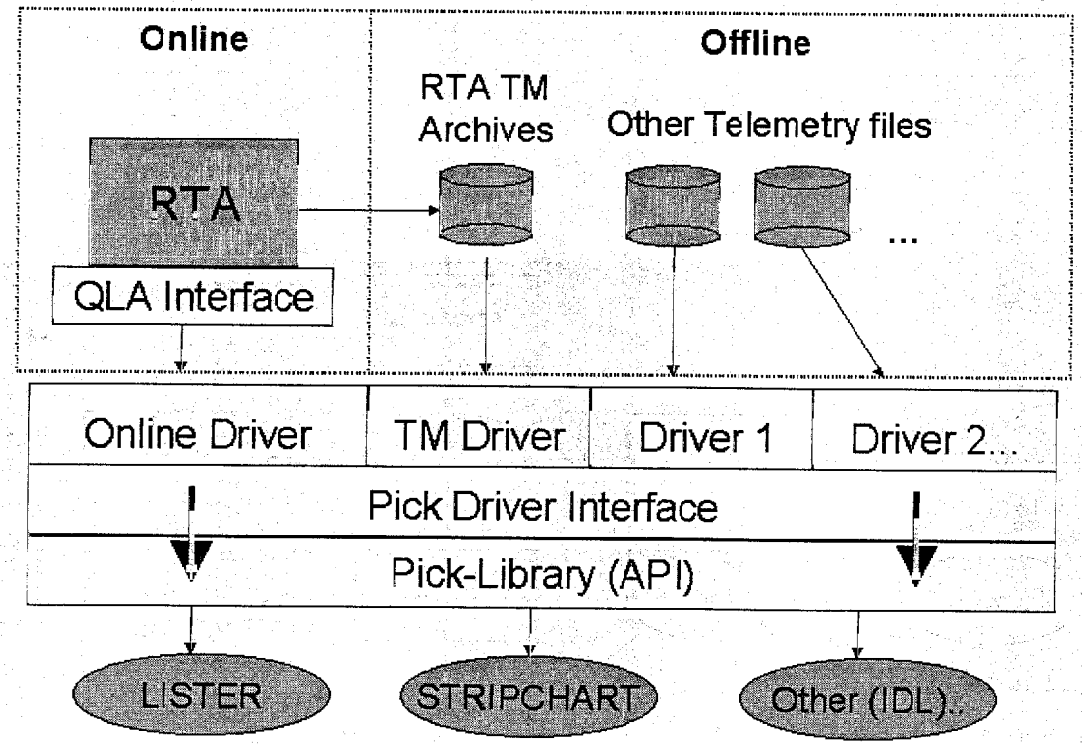
EQ-S Command Console - Overview



EQ-S Command Console - Features

- Access Control with individual passwords for different instruments.
- Text & command based user interface.
- Scripting and batch commanding.
- Memory patch/upload capability (IPCH).
- Communication of Command Console with Command System is based on DECNet objects.

RTA/QLA Pick-Interface - Overview

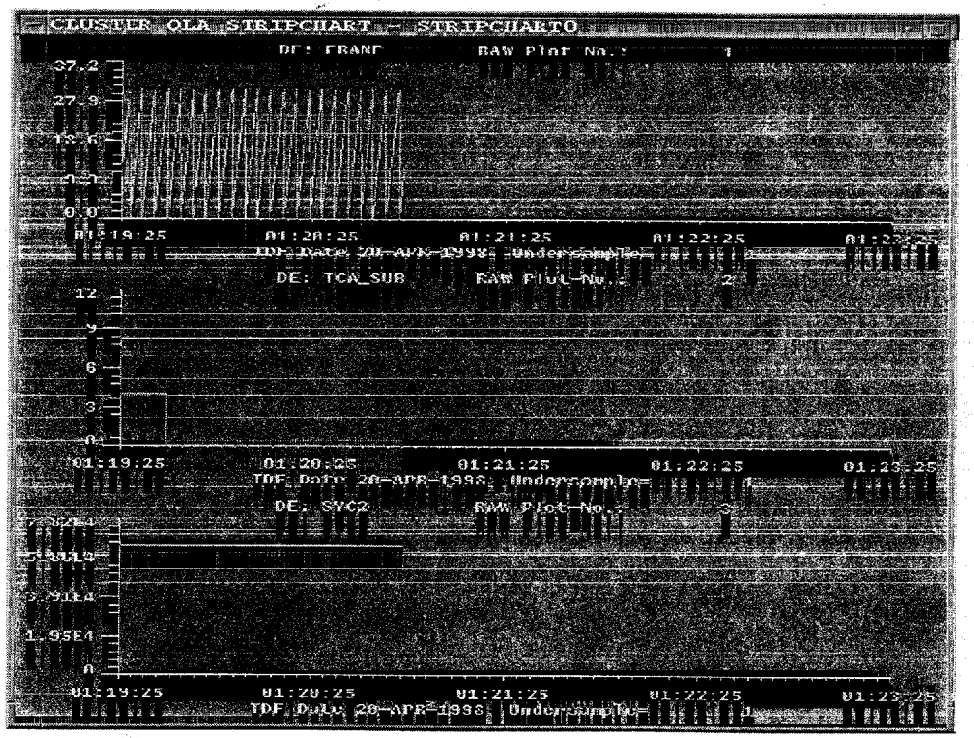


QLA Lister - List Telemetry Items

```
MPECL4 >> lister syc2/hex frame tca_sub
CLUSTER-QLA                          PARAMETER-TABLE                    PAGE: 001

Time                        SYC2          FRAME         TCA_SUB
-------------------------------------------------------------------------------
20-APR-1998 01:21:20.85     FE6B              4               0
20-APR-1998 01:21:20.85     FE6B              4               0
20-APR-1998 01:21:20.98     FE6B              5               0
20-APR-1998 01:21:21.10     FE6B              6               0
20-APR-1998 01:21:21.23     FE6B              7               0
20-APR-1998 01:21:21.35     FE6B              8               0
20-APR-1998 01:21:21.48     FE6B              9               0
20-APR-1998 01:21:21.60     FE6B             10               0
20-APR-1998 01:21:21.73     FE6B             11               0
20-APR-1998 01:21:21.85     FE6B             12               0
20-APR-1998 01:21:21.98     FE6B             13               0
20-APR-1998 01:21:22.10     FE6B             14               0
20-APR-1998 01:21:22.23     FE6B             15               0
20-APR-1998 01:21:22.35     FE6B             16               0
20-APR-1998 01:21:22.48     FE6B             17               0
```

QLA Stripchart - Plot Telemetry Items

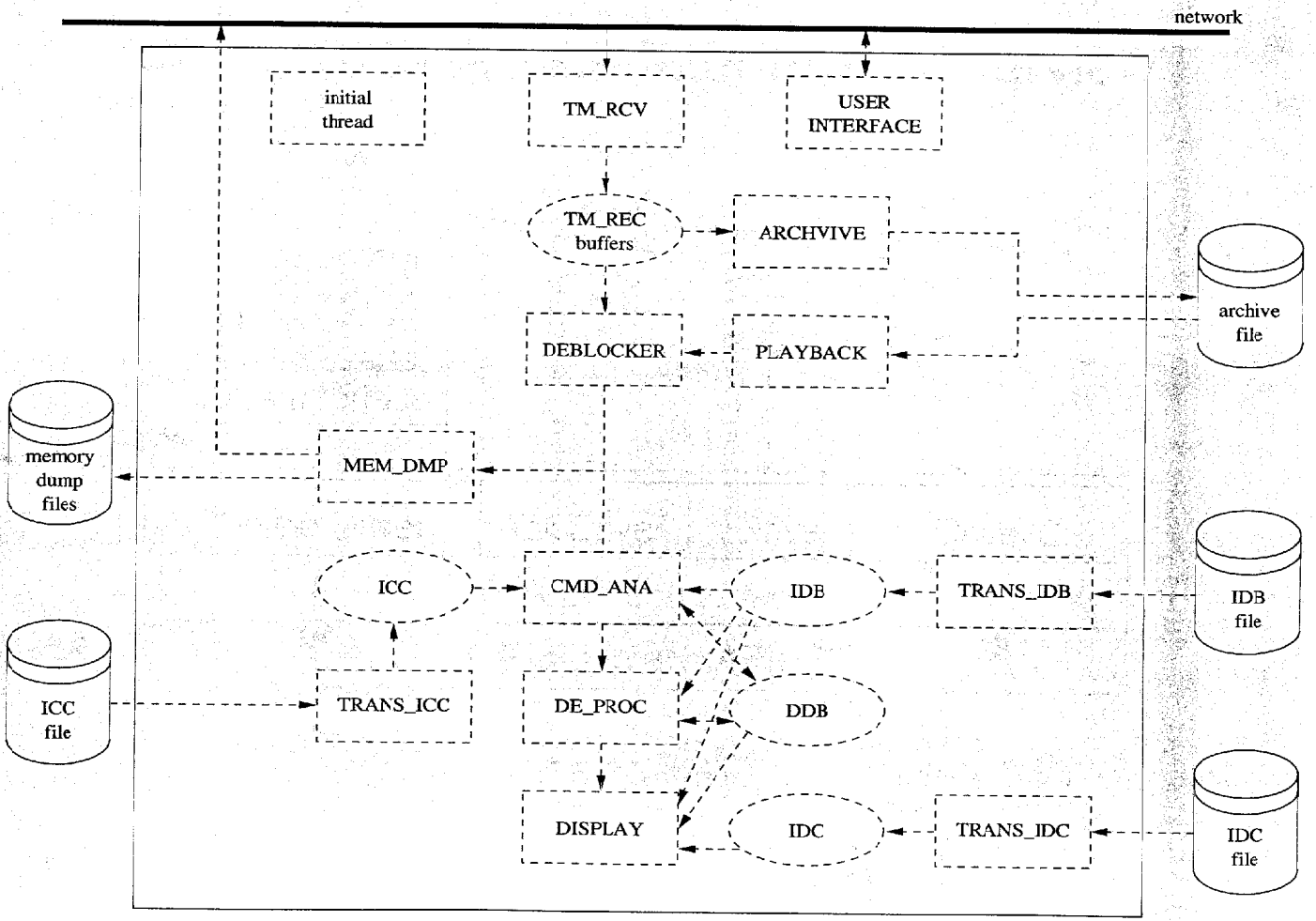


Current state of the RTA

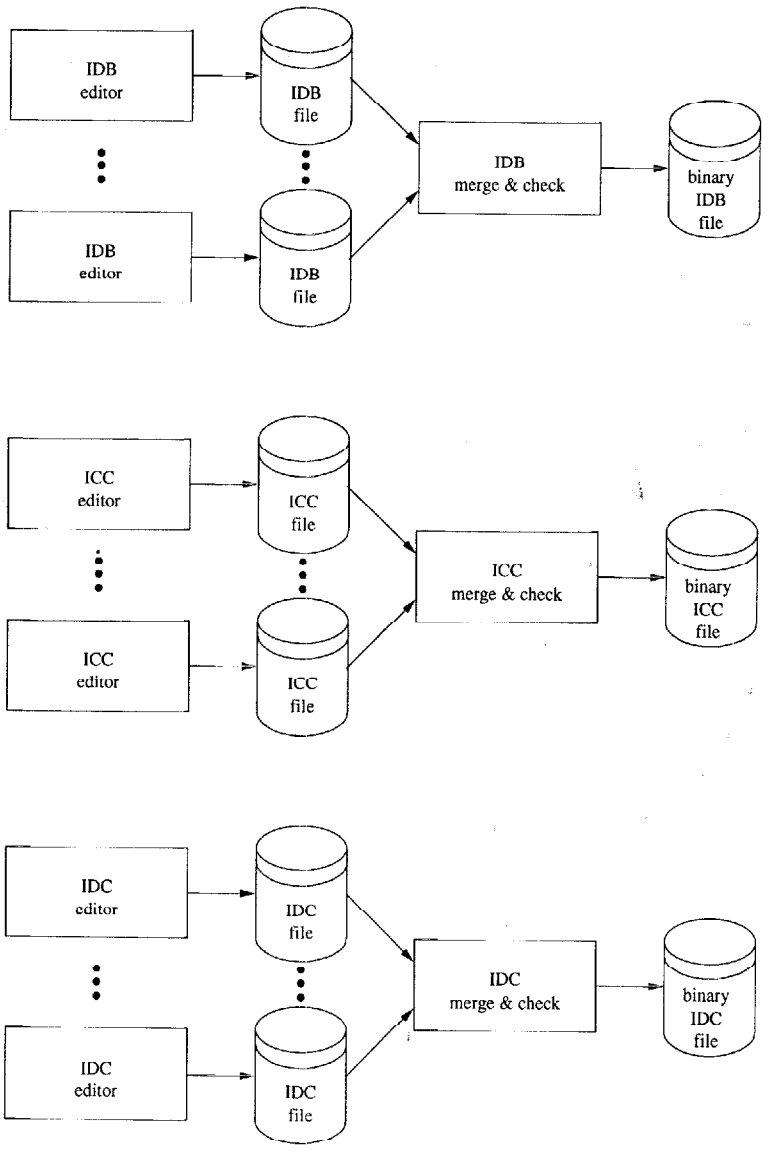
Current RTA software is implemented on OpenVMS systems. The programming language is FORTRAN 77 with extensions supplied by DEC.

- separate processes
  - —priority of different processes can be adjusted
  - —single process failure may not influence other systems
  - —clear interface to make it easier to develope the software in a team
- installed global shared memory buffers to share data between the processes
- global event flags (OpenVMS) to synchronize the processes
- mailboxes (OpenVMS) to transfer messages between the processes
- shared library dynamically linked during execution of RTA for special "action" routines
- software library supplied with OpenVMS to handle terminal screen layout (SMG)
- OpenVMS condition handling
  - —to signal RTA messages (out-of-limits, command errors, requested logging ...)
  - —to handle software errors avoiding the crash of the process
- DECnet as interface to the network
- software configuration control using CMS and MMS
- any number of DISPLAY processes are possible

Online processes, files and commons of the future RTA



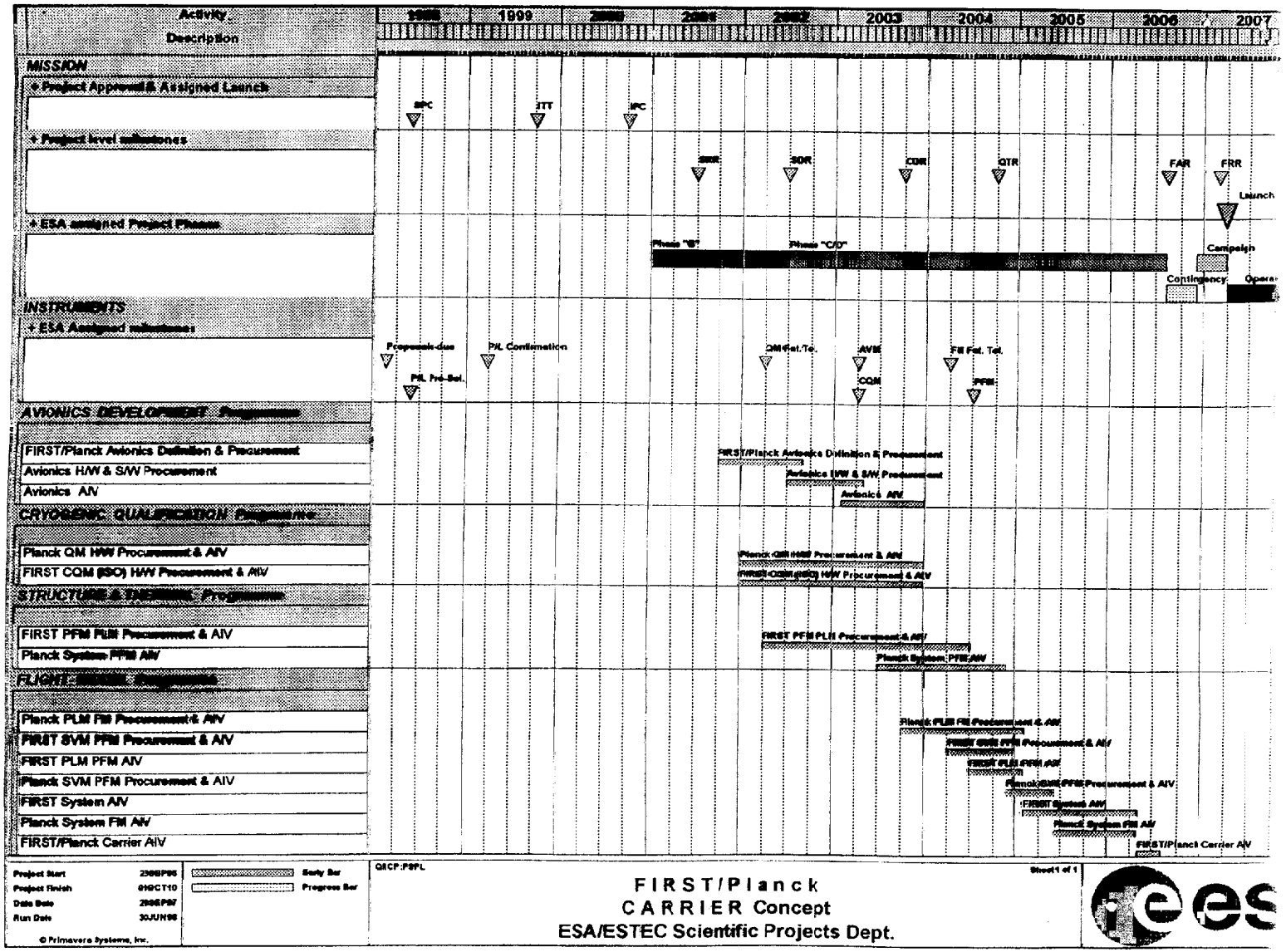
Offline processes and files of the future RTA



Future directions for the RTA

RTA software shall be implemented on U*X systems, if possible on OpenVMS systems too. The programming language will be C.

- using POSIX threads
  - —priority of different threads can be adjusted
  - —single thread failure may not influence other threads
  - —critical threads can be monitored and be restarted in case of a failure
  - —thread interface can be used to synchronize the threads
- no installed global shared memory buffers to share data between the processes are necessary
- BSD sockets as user interface to a RTA process which executes in the background or on a remote host
- shared library dynamically linked during execution of RTA for special "action" routines (dlopen, dlsym, dlclose)
- C runtime library "curses" to handle terminal screen layout
- TCP/IP as interface to the network
- more than one DISPLAY thread is possible
- QLA interface via archive files
- database file (IDB, IDC and ICC) format shall be more flexible


Activity Description
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
MISSION
+ Project Approval & Assigned Launch
+ Project level milestones
+ ESA assigned Project Phases
INSTRUMENTS
+ ESA Assigned milestones
AVIONICS DEVELOPMENT Programme
FIRST/Planck Avionics Definition & Procurement
Avionics H/W & S/W Procurement
Avionics AIV
CRYOGENIC QUALIFICATION Programme
Planck QM HW Procurement & AIV
FIRST CQM (SIC) HW Procurement & AIV
STRUCTURE & THERMAL Programme
FIRST PFM PLM Procurement & AIV
Planck System PFM AIV
FLIGHT MODEL Programme
Planck PLM FM Procurement & AIV
FIRST SVM PFM Procurement & AIV
FIRST PLM PFM AIV
Planck SVM PFM Procurement & AIV
FIRST System AIV
Planck System FM AIV
FIRST/Planck Carrier AIV
IPC
ITT
MPC
SRR
SDR
CDR
QTR
FAR
FRR
Launch
Phase "B"
Phase "C/D"
Campaign
Contingency
Proposals due
PAL Pre-Sel.
PAL Confirmation
QM Rel.Te.
AVM
CQM
FM Rel. Tel.
PFM
Project Start 29SEP95
Project Finish 01OCT10
Data Date 29SEP97
Run Date 30JUN98
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Early Bar
Progress Bar
QICP:FSPL
Sheet1 of 1
FIRST/Planck
CARRIER Concept
ESA/ESTEC Scientific Projects Dept.

FIRST/Planck

2nd Commonality Working Group Meeting

08/07/98 @ESTEC (Ca327)

FINDAS

Status

History

- Start of FINDAS prototype activities -- K.O. ESTEC 28.01.98
- End Phase-1 (Analysis) Presentation by VEGA @ESTEC

  Phase-2 Kick-Off: 04.06.98
- Formal Authorisation to proceed: 10.06.98
- Deadline for comments on Phase 1: 15.06.98

Progress since 4th June

- 9 detailed sets of comments received by deadline (see appendix)
- Feedback extremely constructive - (one exception)
- Several comments/suggestions must be deferred to post-prototype activities
- All points noted but **no** update of documents issued in Phase 1
- All phase 1 documents now at issue 1 (publicly available at http://estsa2.estec.esa.nl:1081)
- Consolidated list of comments issued to VEGA on 1 July 1998
- VEGA answers on 15 July 1998 - availability as above
- Preliminary list of major points presented today

Progress since 4th June (cont'd)

- Tutorial document to be issued by ESTEC Sept. '98 covers middleware, data mining, private test database, etc. Final 12/98
- O2 data base licence (cost = 35.000 £ UK) purchased by VEGA
- CORBA licencing approach agreed with VEGA
- IONA/Orbix (cost = 10545 $ US) to be purchased by ESTEC, transferred and installed at VEGA
- O2 Corba licence (cost = 450 £ UK) purchased by VEGA (re-allocation of budget)
- H/W and S/W configuration for prototype discussed and agreed (JJM, KB, VEGA)

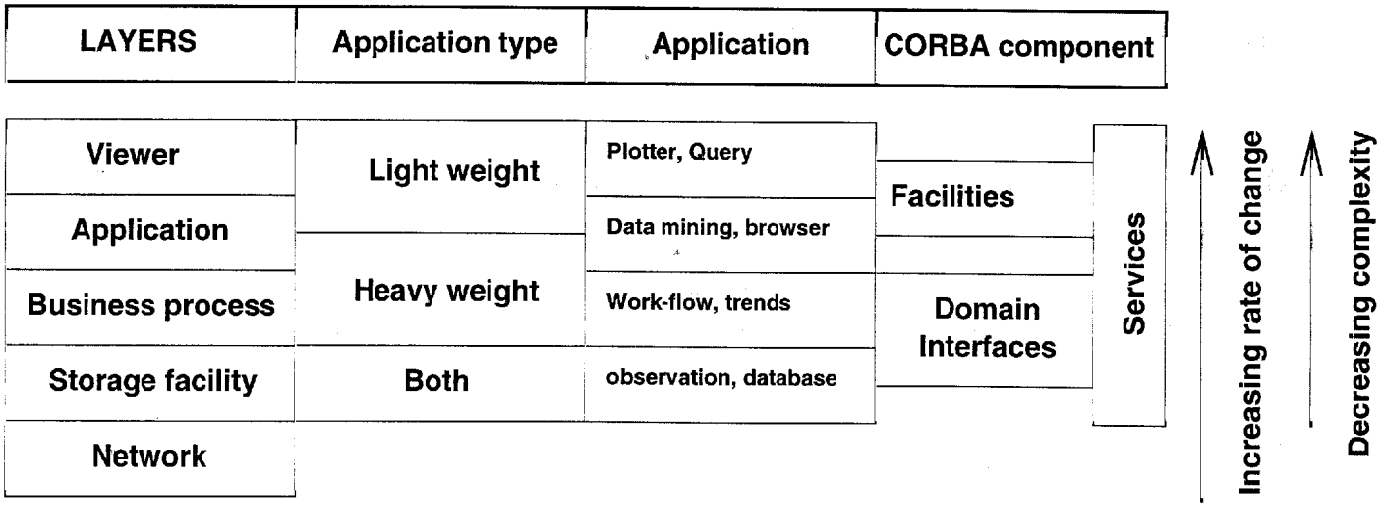
Progress since 4th June (cont'd)

- XMM Archive Management System (AMS) SRD made available to VEGA (from ESOC)
- Agreement with VEGA to include third party application client in prototype implementation - details TBD
- Next progress meeting @ VEGA (11.08.98) T + 2 months
- VEGA to consult IONA re-availability of Orbix for FORTRAN, IDL and C -- due date: 01.08.98
- VEGA have accepted to have one FIRST ICC representative and one Planck/IDIS representative to follow-up Phase 2 but:
  - single interface (PE + JJM) for VEGA
  - continuity in the representation is essential!

Appendix -List of Comments received on 15.06.98

- 13.05.98 Comments by Roelfsema (HIFI), Bauer (PACS) and King (SPIRE) on VEGA "technical proposal - given to VEGA on 14.05.98
- 03.06.98 Comments by C. Arviset (ISO PMA implementation)
- 09.06.98 Kevin Bennet (IDIS/ESTEC)
- 13.06.98 F. Pasian (IDIS/LFI)
- 15.06.98 W. O'Mullane (IDIS/ESTEC)
- 15.06.98 M. Merri (ESOC / XMM AMS)
- 15.06.98 R. Walter Obs. Geneva (Integral ISDC)
- 15.06.98 P. Roelfsema (FIRST/HIFI)
- 17.06.98 O. Bauer et al (FIRST/PACS)

CORBA based architecture



CORBA and OO technology

- Management of complexity
- Eases scalability
- Eases evolution of system

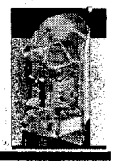
but it needs:

- Strong architecture
- Well trained developers
- A strict development discipline

Recommendation: Hire a company specialized in the development of large distributed objects architecture to get a solid base as well as training and mentoring.

Characteristic	Grade	Comment
Reliability and Integrity requirements		
Data integrity	High	
Referential integrity	High	
24x7 operation	High	
Failure recovery	High	
Data model requirements		
Complex relationships	High	Networks of objects with many-to-many relationships
Composite objects	High	refers to structural hierarchies of components
Large objects	Medium	$\geq$10 Kbytes
Small objects	High	$\approx$100 bytes
Modifiable schema	High	
Transaction requirements		
Many readers per object	Low	
Many writers per object	Low	
Long transactions	Medium	
Short transactions	High	
Large transactions	Medium	
Small transactions	High	
Distribution requirements		
Many clients	<1000	
Many databases	<50	
Many sites	<10	
Heterogeneous platforms	Medium	
Flexible configuration	High	
Performance requirements		
Scalability	Medium	
Reading objects	High	
Traversing relationships	High	
Updating objects	Medium	
Executing methods	High	
Making queries	Medium	
Environment requirements		
Standards support	High	

Table 1: Data model requirements



FINDAS : prototype evaluation by end-users/FSC-ICCs

- Both FSC and ICC involvement needed : hands-on experience, usefulness and capabilities.
  - → **"What can we do with FINDAS, what can FINDAS do for us ?"**
- FINDAS = OODBMS-"enabling tool" to use, provides framework around which to develop.
- Test-clients with OO-methods have to be written for prototype validation.
- These test-clients must perform simple operations, e.g. adding, changing and deleting objects, merging objects, adding information to objects, pulling out a bytestream, etc.
- It is not the purpose to generate full OO-models, real-life or extensive applications.
- Test-clients should be simple and concentrate on the following questions :
  - → How to develop and integrate harmoniously with FINDAS ?
  - → How FINDAS can be of use for a later Ground Segment ?
  - → How does the interface with FINDAS work in practice ?
  - → Is the FINDAS-prototype really useful for the END-USERS ?

Prototype evaluation support and exchange

- ICCs will receive a document from ESA (Oct 1998) with information HOWTO :
  - → interface with FINDAS
  - → use the OO-database scheme of the prototype

  providing INFORMATION about :
  - → the OO-system architecture of the FINDAS-prototype, its limitations and capabilities
  - → requirements to which client-applications must comply in order to talk to FINDAS
  - → purpose and scope of the validation of the prototype
  - → the OO-database scheme
- ICCs will be asked to provide test-proposals with details about the "clients" they will implement and deliver this info to ESA-personnel involved from FSC, EM and Project.

Prototype evaluation support and exchange (cont'd)

- ICCs will come to the ESTEC site to develop, run and test their "clients".
- ICCs will inform ESA of problems, difficulties, challenges encountered.
- The end-users will provide a prototype **evaluation report** at the end of prototype evaluation.
- Schedule :
  - "Proposals" : before Xmas 98
  - FINDAS prototype delivery : Feb 99
  - Testing period : ~ Mar 99 - Jun 99
  - Decisions about "real" FINDAS : to follow

FIRST science ground segment document management

- Need for efficient exchange (within and between institutes including ESA) of documents already a fact
- Eventually we plan to do this through FINDAS - but need something now
- The DMS system (initially used internally by ESA projects) is available now
  - DMS is accessed through the WWW (e.g. Netscape)
  - Allows several 'projects' with different access right (e.g. private pages)
  - Can be replicated for efficiency
- Adopted (cloned) by Planck instrument teams
  - 'Master' site at ESA SCI-SA, currently replicated at MPA, Garching
  - Simple 'rules', administered by ESA SCI-SA as 'service'
- Propose to adopt DMS for FIRST instrument/ICC teams and FSC for now
- Later access through FINDAS