FIRST/ESA/M/0038.10

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From: OHB@MPEPL.PLASMA.MPE-GARCHING.MPG.DE (by way of Ken King <K.J.King@rl.ac.uk>)
Subject: Minutes of Commonality Meeting in Paris, 13-Nov-1997

From : O.H. Bauer, FIRST-PHOC, MPE Garching

To :		
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Date : 27-Oct-1997

Ref : FIRST/PHOC/CWG/97-001/Em

Subject: FIRST/Planck Digital Electronics and Commonality Meeting,
Paris, 13-Nov-1997, 9:00-17:00 LT at ESA Headquarters

Dear FIRST/Planck Colleagues,

the Announcement of Opportunity for the combined FIRST/Planck mission has been released beginning of October and the different groups are starting to work on their answers to the AO.

Obviously we are in the very favourable position that for all three FIRST instruments our Italian colleagues are willing to provide the digital electronics and related H/W and S/W components.

In addition the Planck HFI/LFI groups have dicussed the possibility to go in the same direction.

This common approach concerning the digital electronics could open a wide area of communality and could be an important cost saving factor for the FIRST/Planck Project.

In order to probe and discuss the different commonality aspects, starting from the digital electronics (DPU) as the central part, I would like to organize a one-day meeting at ESA Headquarters, Paris, on Nov 13, 9:00-17:00 LT.

The following points should be addressed:

(1) Digital electronics
Each team could give a short presentation concerning the overall concept, interfaces and modes of operation.
(2) Spacecraft interface simulator
(3) On-board microprocessor(s)
(4) On-board programming language

(5) Software development environment and standards
(6) Software validation facilities
(7) Instrument on-board software including instrument autonomy
(8) Memory load and verification
(9) Instrument commanding: Instrument Command Sequences (ICS's), Macros
(10) Instrument software simulator
(11) Instr. EGSE: Real-Time Assessment (RTA), Quick-Look Analysis (QLA)
(12) Test sequence language
(13) Commonality between Instrument Level Tests (ILT), System Tests and Operations
(14) FIRST Integrated Network and Data Archive System (FINDAS)

Please confirm your participation by Tuesday, Nov 4.

Comments on the meeting itself and the proposed agenda are welcome.

Best regards, Otto H. Bauer

Minutes of the meeting

(Peter Roelfsema, 25/11/97)

1 Introduction

People present:

OHB; general mission considerations (Appendix);

2 DPU outline (IFSI)

Appendix

Some 80x86 is the preferred CPU to use. The Marconi 31750 processor seems to be out already (to be discussed later). Poglitch proposes to look into the NASA qualified list (which goes up to a 80486 which is radiation qualified up to 100 Krad).

Not clear whether LFI will be done in this fashion, LFI may build in-house.

Total cost for all instruments (PHOC, BOL, HET, HFI) about 3.6 Mpounds.

Timing of deliveries could be difficult since all groups need the boards+S/W at roughly the same time. This can be partly fixed by involving industry.

3 LFI
Appendix

Looks into using the MA31750, apparently ESA is looking into (intending to) using it for the FIRST SVM.

LFI has high data rate, and requires a compression factor of 7.5 to get down to the rate allocated to it

(about 8kb/s)

Proposals for processors to use for DPU and dedicated compression DSP.

4 PHOC

Appendix

Data compression unit will be really important; CRE generates 1.6Mb/s! PHOC foresees this unit NOT to be part of the DPU.

Master clock signal is needed, but it has to have enough resolution/accuracy to be useable by the PHOC CRE.

Likely PHOC's data rate varies somewhat with time, with as a result that the rate from data compressor to DPU can be higher than 40kb/s at times. This means some work will have to be done in the DPU,. and requires memory in the DPU for intermediate data saving. Commonality here has to be investigated.

Uplink requirements for compression software are quite significant!

5 HET (HiFi)

Appendix

Also for HiFi the 2Kb/s for 2hr is tight in terms of the amount of data to be uplinked.

6 HFI

Appendix

Required compression factor is about 5.

Breadboard compression unit is made now, using TI805 transputer.

For programming language no decision, ADA and C are possibilities. OS on the CPU has to be discussed (will come later).

7 ROI

Appendix

Large(r) number of detectors -> need compression too. Data are probably deglitched in real time.

For the FTS data analysis for signal conditioning requires short term storage and buffering memory (of order 10 or a few 10Mbytes).

8 Initial conclusion of different presentations

Commonality options for

- Chopper
- Data compression. unit/algorithms/environment
- DPU

9 Commonality issues

9.1 Which micro processor

HS reports that selection will be made by end of the year:

- 31750; well documented, well known, but. going out of production
- 486 version; is not qualified yet, but is under study by ESA
- SPARC V7 (32 bit); is under development, looks good. Currently a 3 processor implementation. Is likely to be too late.

Likely the choice will be between 31750 and 486.

Languages; C is option. At ESTEC investigations are ongoing for this (Appendix 8)

The NASA list is brought up; according to HS in principle this should be applicable. HS will check this at ESTEC.

9.2 S/C interface simulator

Appendix

All would like PC interface board, but who designs and makes it.

Basic design could be like ISO-SWS setup:

Instrument PC(with interface board)ethernetESGE commanding unit

9.3 Telemetry issues

Use package telemetry, but separate science and house keeping.

MOC should be able to monitor health and safety by only looking at house keeping packets. HK data should not be compressed.

A few lines will be made available for reading out data from an un-powered instrument (e.g. temperatures).

9.4 Programming language/soft ware

Lot of interest for C.

Possibly (likely) some assembly will be required.

Data compression software could be of common design.

9.5 Software development environment/standard

Standard for small projects is applied for onboard software

9.6 Software validation facilities

In the project team a person will be (hopefully) appointed to be knowledgeable about various software systems in use for FIRST on board software issues.

9.7 Instrument simulator

Appendix

A good possibility would be to use a combination of hardware and software; a hardware DPU with a software model for the analog part(s) of the instrument.

Electrical model versions of the DPU could be used for this purpose.

Same setup could then be used for software validation, EE tests and ground segment testing/simulation

9.8 Instrument autonomy

Instruments need to decide what they need.

Power off request has to go to OBDH, so it can switch instrument off.
Clearly the mechanisms for such operations can be common.

Likely the satellite will monitor e.g. currents flowing to the instrument and act on limits on that.

SVM memory will be ably to take 48 hrs (TBC) of data. This opens interesting options for e.g. PHOC/BOL parallel survey work at higher data rate. A long discussion followed with no clear results, but a number of open questions; what can this memory be used for, what about uploading schedules for 48 hours observing, can this large amount of memory be filled at higher rates??

9.9 Memory load and verification

.much discussion about loads.

How are memory loads checked? Single checksum? Checksum is done by OBDH, likely the instrument needs to check this back once it got there.

Memory dumps will be needed.

SOHO has 1Gbit memory, with roughly 1 error/minute! So error correcting routines are essential.

9.10 Instrument commanding, ICS's, macro's

In instrument we need atomic building blocks with a few/simple parameters to command subsystems (ISC - Instrument Command Sequence in ISO). These can be used early on in testing, and thus verified early on.

Macro's can be generated by combining a number of these atomic blocks.

9.11 Instrument operational modes

Appendix

Suggested are (especially for FIRST); primary, serendipity, partner, standby, sleep, off and test.

Additions could be; safe, memory load and parallel modes.

Data transfer rate and polling strategy between OBDH and instruments is unclear at this time. Burst modes may be involved..

9.12 Instrument EGSE, RTA/QLA

Appendix

PHOC can provide (0.5 manyear effort) upgraded, OS independent version of RTA/QLA environment (in use for ISO, Equator-S, CLUSTER).

9.13 Testing; sequences, language

Will (mostly) be addressed by document to be released shortly by Pierre Estaria

9.14 FINDAS

Appendix

Big aim; does everything for everybody at all times.

10 Conclusions

- IFSI writes DPUsatellite communication software
- Need space craft simulator fairly soon!
- A number of commonality issues can be looked at in the ESA-CWG, but it needs support form the instrument groups
- EGSE/RTA/QLA hardware should be decided in about a year, PHOC will describe available system in more detail. Following this agreements can be made on OS and porting it to that OS.

Action items

CWG#1-1 - HS - check whether processor from NASA list can be used

CWG#1-2 - HS - find out what code validation/test validation tools are meant in the small projects standard document

CWG#1-3 - ?? - review use of available on board memory for different operating modes at higher data rates, allowing for longer down link time.

CWG#1-4 - all - identify key personnel within instrument groups to join commonality tiger teams on e.g. data compression hardware/software, EGSE setup, RTA/QLA etc. etc.