# HERSCHEL/PACS

## SPU HIGH LEVEL SOFTWARE
## User Requirement Document

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# 1. Introduction

The Herschel Space Observatory[1] is the fourth cornerstone mission of the European Space Agency (ESA) `Horizon 2000' science plan. It will be implemented together with the Planck mission as a single project. The Herschel Space Observatory will perform photometry and spectroscopy in the 60-670 μm wavelength range (RD004). It will have a radiatively cooled telescope and a payload complement of three instruments housed inside a super fluid helium cryostat, ``HIFI``, ``SPIRE`` and ``PACS`` developed by three consortia. The Institute of Computer-Aided Automation (Pattern Recognition and Image Processing Group) from TUVIE, the Institute of Astronomy from UVIE and Joanneum Research from Graz are parts of the '**P**hotodetector **A**rray **C**amera **S**pectrometer' PACS Instrument Development Team. They are responsible for developing and implementing data compression algorithms on a very integrated and radiation tolerant digital signal processor based on the TSC21020E architecture for space application and ensuring the communication with the warm electronic sub-units.

## 1.1. Purpose of the Document

This document defines the user requirements of the SPU High Level SoftWare. The user requirements in a software development lifecycle are the result of the problem-understanding phase and reflect the needs of the customer who will finally utilize the software.

The Signal Processing Unit (SPU) is one of many subsystems of PACS. It will be provided by IAC and UVIE/TUVIE. The tasks are split in two categories: HW+Low Level SoftWare development (IAC) and High Level SoftWare (UVIE/TUVIE). The HLSW development is the application SW and the communication interface software, and all the rest is the HW+LLSW.

[1] The previous name of Herschel Space Observatory was the Far InfraRed and Submillimeter Telescope 'FIRST'

## 1.2. Acronyms and Abbreviations

| | |
|---|---|
| ADSP | Analog device DSP |
| AID | Activity ID |
| AOCS | Attitude and Orbit Control Subsystem |
| ASW | Application SoftWare |
| BOL | BOLometers |
| CDMS | Command and Data Management System |
| CPU | Central Processing Unit |
| CRE | Cold Readout Electronics |
| CSL | Centre Spatial de Liège |
| DEC/MEC | Detector Controller/Mechanisms Controller |
| DPU | Digital Processing Unit |
| DRCU | Detector Readout and Control Unit |
| DSP | Digital Signal Processor |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| FCU | FPU Control Unit |
| FIRST | Far Infrared and Sub-millimeter Telescope |
| FPU | Focal Plane Unit |
| HIFI | Heterodyne Instrument for HERSCHEL (HiFi instrument ) |
| HK | House-Keeping |
| HLSW | High Level SW |
| HS | High Speed |
| HSO | Herschel Space Observatory |
| HW | HardWare |
| I/F | Interface |
| IAC | Instituto de Astrofísica de Canarias |
| ICC | Instrument Control Centre |
| ID | Identification |
| IFSI | Istituto di Fisica dello Spazio Interplanetario |
| JR | Joanneum Research |
| LLSW | Low Level SW |
| LSB | Least Significant Byte |
| LWL | Long WaveLength |
| MFCU | Mechanisms and Focal plane electronics Control Unit |
| MSB | Most Significant Byte |
| OBCP | On-Board Control Procedure |
| OBS | On-Board Software |
| PACS | Photodetector Array Camera and Spectrometer |
| PHC | PhotoConductors |
| PMA | Program Memory Address |
| PMD | Program Memory Data |
| PRIP | Pattern Recognition and Image Processing |
| PROM | Programmable Read Only Memory |
| RAM | Random Access Memory |
| ROM | Read Only Memory |
| SAU | Smallest Addressable Unit |
| SID | Structure ID |
| SPIRE | Spectral and Photometric Imaging Receiver |
| SPU | Signal Processing Unit |
| SW | SoftWare |
| SWL | Short WaveLength |
| TBC | To Be Confirmed |
| TBD | To Be Defined |
| TBU | To Be Updated |
| TBW | To Be Written |
| TM | TeleMetry |
| TUVIE | Technical UVIE |
| UR | User Requirement |
| URD | User Requirements Document |
| UVIE | University of Vienna |
| WE | Warm Electronics |

## 1.3. References

### 1.3.1. Applicable Documents

| | | |
|---|---|---|
| AD001 | PACS-TW-GS-001 | HERSCHEL/PACS SPU High Level Software Specification Document |
| AD002 | PACS-TW-PL-001 | HERSCHEL/PACS SPU HLSW Development Plan |
| AD003 | PACS-TW-ID-001 | HERSCHEL/PACS SPU HLSW to DPU Interface Description |
| AD004 | PACS-IC-RD-001 | PACS SPU Start-Up SW and LLSW Drivers URD |

### 1.3.2. Reference Documents

| | | |
|---|---|---|
| RD001 | BSSC(96)2 | Guide to Applying the ESA Software Engineering Standards to Small Software Projects |
| RD002 | IFSI/OBS/PL/2000-001 | DPU/ICU On Board Software Product Assurance Plan |
| RD003 | FPL-IC-1214-01-CRS | Herschel PACS SPU HW-SW Interface Control Document |
| RD004 | SCI-PT-IIDB/PACS-02126 | HERSCHEL/PLANCK Instrument Interface Document - Part B – Instrument “PACS” |
| RD005 | PACS-IC-RS-001 | PACS SPU Hardware Requirement Specification |
| RD006 | PACS-ME-PL-005 | Operating Modes of the PACS Instrument |
| RD007 | SCI-PT-ICD-7527 | Packet Structure – Interface Control Document. FIRST/Planck Project |

## 1.4. Overview of the Document

The URD of the SPU HLSW is structured as follows:

- In Section 1, an introduction and the software statement are presented. It contains a short overview of the PACS project, and the main contribution of the UVIE and TUVIE.
- In Section 2, the general constraints of the HLSW and its operational environment are given.
- Section 3 contains the specific requirements upon which the SPU HLSW will be accepted.

# 2. General Description

## 2.1. General Capabilities

PACS will contain two SPUs: one nominal and one redundant. Only one sub-unit will be switched on at a time. The redundant SPU will be switched on whenever a failure occurs to the nominal one. This document focuses on the SPU HLSW description, which consists of the data reduction and compression software (the application SW) and the communication interfaces with DEC/MEC and DPU. The dialogue mechanism of the SPU OBS with the other subsystems is depicted in Figure 1. Basically, two CPU boards are represented, which work independently. They are called SWL SPU and LWL SPU. The HLSW will be implemented in both CPUs. Two links are represented for each CPU:

- Raw data link, which transfers the data information from DEC/MEC.
- Compressed data and Command/Response link, which transfers the compressed data information, the responses and HLSW HK data from SPU to DPU and commands from DPU to SPU.

Each CPU will receive its own raw data and its own commands independently and it will send its own responses and its own HLSW HK. The main task of the SPU HLSW is the data reduction and compression in order to achieve the desired downlink rates. Indeed, several compression modes designed to operate at various environmental conditions will be implemented.

## 2.2. Detectors Description

The PACS instrument will perform imaging photometry and imaging spectroscopy. In photometry mode, it will use bolometers for imaging, while photoconductors will be used in spectroscopy mode. The switch between both detectors will be performed by the DEC/MEC under DPU command. Therefore, the raw data behaviour and size will depend on the used observing mode. The data compression SW will operate upon these consequences.

The detectors characteristics are as described below.

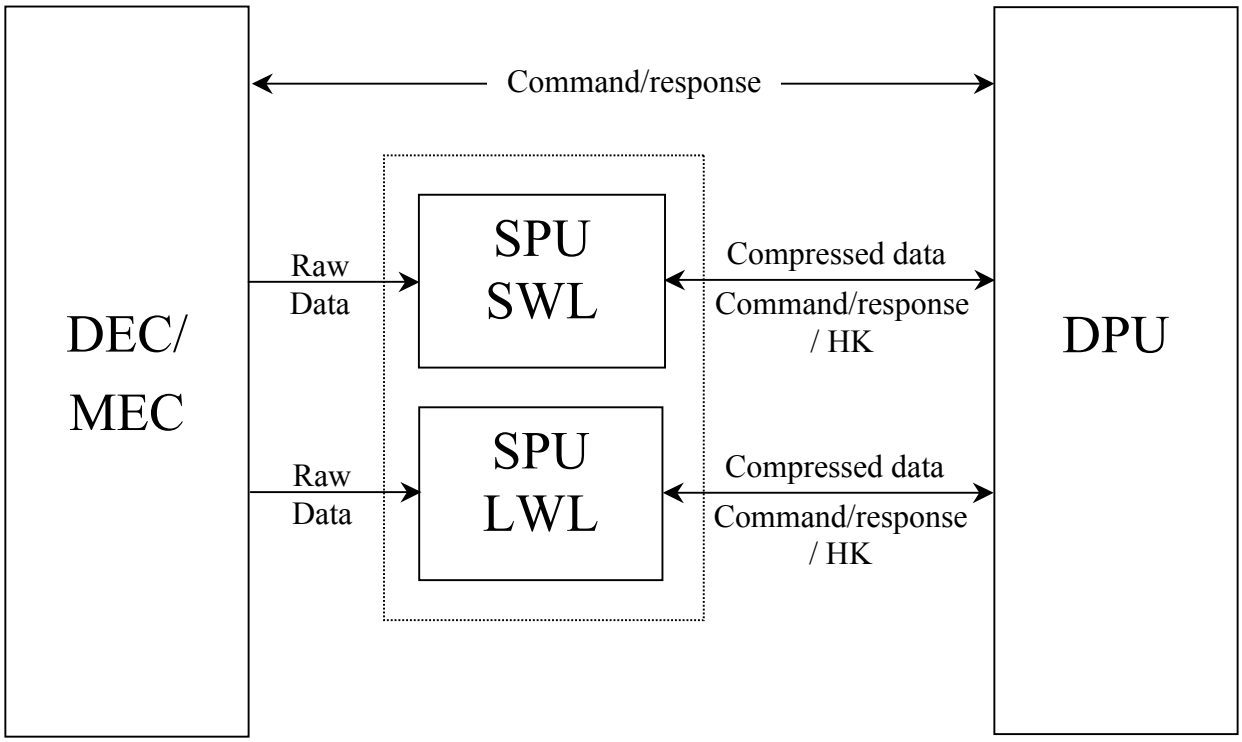


*Figure 1. Communication Links between SPU OBS and Other Subsystems*

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### 2.2.1. Bolometers in Photometry

- 8x(16x16) pixels for the SWL photometer
- 2x(16x16) pixels for the LWL photometer
- Maximum sampling rate is 40 Hz
- 16 bits to code each sample
- The resulting raw data flow is 1600 kbit/s in nominal case
- 4 samples to average in nominal case
- The fastest chopping with 1 sample/10 Hz
- Glitch rate 0.1 Hz per pixel
- Glitch tail < 0.33 s

### 2.2.2. Photoconductors in Spectroscopy

- (16x25) pixels for the SWL spectrometer
- (16x25) pixels for the LWL spectrometer
- 1 empty column is added from DEC/MEC to each array
- 2 rows are added for test purpose to each array
- Sampling rate is 256 Hz
- 16 bits to code each sample
- The resulting raw science data flow is 3744 kbit/s
- Reset interval is between 1/32s and 4s
- 8 samples per ramp in the most challenging case
- Glitch rate 0.1 Hz per pixel
- Glitch tail < 0.5 s

## 2.3. General Constraints

### 2.3.1. Software Constraints

- Telemetry rate for the science data is 120 kbits/s averaged over 24 hours (RD004).
- Burst mode is limited to 300 kbits /s for up to 30 minutes (RD004).
- The packet block should fit into one telemetry packet (RD007).
- CPU clock speed is 18 MHz (RD005).
- Maximum sampling rate of 40 Hz in photometry
- Sampling rate of 256 Hz in spectroscopy
- The reset interval is between 32 Hz and ¼ Hz for a sampling rate of 256 Hz in spectroscopy
- For a science data size of 480 kBytes in photometry or 468 kBytes in spectroscopy (see AD001), the typical compressed entity size per board is respectively about 30 kBytes[2] or 12.5 kBytes[3].

[2] The number of 30 kBytes is obtained by dividing the 480 kBytes by 16. 16 represents the minimum compression ratio to achieve in photometry in order to fulfill the telemetry rate of 100 kbits/s

[3] The number of 12.5 kBytes is obtained by dividing the 468 kBytes by 37.44. 37.44 represents the minimum compression ratio to achieve in spectroscopy in order to fulfill the telemetry rate of 100 kbits/s

### 2.3.2. Communication with the DEC/MEC

- The communication with the DEC/MEC is performed via one IEEE 1355/spacewire data link per DSP
- The link speed will be set to a rate of 10 Mbps
- Data are continuously transmitted from DEC/MEC to SPU, which consists of detector raw data and DEC/MEC header
- Specific parameters are attached with each readout (science data) as DEC/MEC header
- DEC/MEC header consists of the data type, observation configuration, the timing parameters, and the compression parameters
- The DEC/MEC raw data packet is as described in AD001
- The SPU does not transmit anything to the DEC/MEC
- The SPU will transmit a DEC/MEC header error message to DPU in the HK, whenever a corrupted DEC/MEC header is received
- The SPU will transmit the link connection status with DEC/MEC in the HK to DPU

### 2.3.3. Communication with the DPU

- The communication with the DPU is performed via one IEEE 1355/spacewire data link per board
- The link speed will be set to a rate of 10 Mbps
- The reduced and compressed entity of science data and DEC/MEC header shall be packaged, split into blocks which fit into the telemetry packets and made available to the DPU
- The compression mode read from DEC/MEC header is set by DPU
- The compression of the science data and DEC/MEC header is described in AD001
- The detector selection tables, which are a part of the compression parameters, are directly sent from DPU to SPU using a write command (AD003)
- The detector parameters, which are mandatory for data pre-processing in photometry and spectroscopy, are directly sent from DPU to SPU using a write command (AD003)
- Command packets are sent from DPU to SPU
- The DPU commands for the SPU HLSW are described in AD003.
- The SPU HLSW acknowledges the command reception and/or execution by sending the command response within a maximum timeout of 200 milliseconds[4].
- The SPU sends the HK data to the DPU at regular time interval compatible with the PACS overall HK rate.

[4] In this case, the maximum data size, which could be dumped, is 10 Kbytes, while only 9 Kbytes could be checked.

- The SPU HSLW HK data are listed in AD003.

### 2.3.4. Interfaces to SPU Low Level SW

- SPU control is split between LLSW and HLSW
- The sequence describing the transition between the LLSW to HLSW for the control of the SPU is defined in AD004.
- LLSW stays in PROM
- The HLSW program shall be loaded from EEPROM to RAM by the LLSW at the Start address defined in the HLSW User Manual.
- The SPU control is handed to the HLSW upon a DPU command to LLSW.

### 2.3.5. Microprocessor (ADSP 21020) Constraints

- The Program Memory Address Bus: 24 bits (RD003)
- The Program Memory Data Bus: 48 bits (RD003)
- Fixed Point and Floating Point data: up to 32 bits of the PMD (Program Memory Data) bus (RD003)
- The clock cycle is 55,6 ns (CPU speed is 18 MHz as described in RD003)

### 2.3.6. Memory Constraints

The operations of the HLSW on the SPU hardware depend on the memory size available. Therefore the data stream coming from DEC/MEC should be adjusted according to the memory requirements for a regular on-board data processing and storage. The following numbers are taken from RD003.

- PROM of 192 kB (32 kW x 48)
- EEPROM of 1,5 MB (256 kW x 48)
- (PRAM of 3 MB (512 kW x 48), DRAM of 2 MB (512 kW x 32)and expended DRAM of 2 MB (512 kW x 32)) per CPU board are available

### 2.3.7. Transmission Modes

The transmission mode, which represents the way the reduction and compression should be done, is read from the DEC/MEC header and on board stored information. It consists of the compression parameter and the detectors' selection information.

Four transmission modes are proposed:

- Compressed Data Transmission Mode
- Raw Data Transmission Mode
- Transparent Mode
- Buffer Transmission Mode

## 2.4. User Characteristics

The natural customer of this SW will be:

- The software engineers, who will follow the unrolling of the satellite lifecycle, performing tests, maintenance of the software
- The ICC personnel responsible of the command, providing the command procedures related to the HLSW parameters to be performed
- The other instrument subsystem developers related to the SPU HLSW

## 2.5. Operational Environment

The SPU dedicated to data reduction/compression receives its input via two IEEE 1355/spacewire data links from the DEC/MEC. The data are developed and processed in the HLSW, according to the DEC/MEC header and tables stored on board. Then, the processed data are transferred to the DPU via two IEEE 1355/spacewire data links. The I/F between SPU HLSW to DPU is specified in AD003.

The HLSW will be implemented on two ADSP 21020 using the following environment as described in RD003:

- The use of the space version of the VIRTUOSO$^{TM}$ operating system.
- The use of the IEEE 1355/spacewire data link and the SMCS 332 high-speed serial link controller chip.
- The use of 7 MB of RAM per board.
- The use of 32 Kbytes of data transfers memory (DPRAM) per board.

## 3. Specific Requirements

The main functions of the HLSW are:

- Acceptance, reception, verification and execution of commands from the DPU
- Get data from the DEC/MEC interface
- Science data acquisition from DEC/MEC I/F including a header containing the data type, the observation configuration and the compression parameters
- Science data reduction and /or compression
- Compression of DEC/MEC header
- Make the reduced/compressed science data and compressed DEC/MEC header available to DPU in the format specified in AD003
- Implementation of the Warm Reset routine
- Implementation of Peak-up SW I/F
- Implementation of SPU Test mode using a synthetic data generated on board
- Implementation of the Bolometer Background Cancelling mode
- Stop and start the compression SW whenever it is required by DPU
- Load and dump to/from RAM
- SPU RAM check
- Write to the SPU RAM

All these functions will induce the following requirements, which will be listed as follows: the switch on requirements, switch off requirements, SW requirements, communication requirements and telemetry rate requirements. These requirements are split between the capability and the constraint requirements.

### 3.1. Capability Requirements

#### 3.1.1. Switch on Requirements

| ID | Requirement |
|---|---|
| **SPU-OBS-ON1** | After a safe switch on, control of the SPU is handed over from LLSW to HLSW. |
| **SPU-OBS-ON2** | The HLSW shall start sending HK to the DPU whenever it has the control over the SPU |

### 3.1.2. Switch off Requirements

| ID | Requirement |
|---|---|
| **SPU-OBS-OF1** | There is no data storage on a memory from HLSW before the switch off of the SPU unit. |

### 3.1.3. Software Requirements

| ID | Requirement |
|---|---|
| **SPU-OBS-SW1** | The SPU HLSW shall perform the reduction and compression procedure according to DEC/MEC header. |
| **SPU-OBS-SW2** | The SPU HLSW shall have the possibility to detect data corruption in the loaded memory area. |
| **SPU-OBS-SW3** | The SPU HLSW shall generate the HK parameters indicating the current compression mode and the results of the reduction/compression process depending on their availability at a data rate compatible with the overall PACS HK. |
| **SPU-OBS-SW4** | The SPU HLSW shall fulfil the DPU instructions requirements especially those concerning the compression parameters. |
| **SPU-OBS-SW5** | The SPU HLSW shall be able to abort data processing whenever a DPU stop command is received. |
| **SPU-OBS-SW6** | The SPU HLSW shall be able to start data processing whenever a DPU start command is received. |
| **SPU-OBS-SW7** | The SPU HLSW shall be able to perform the Warm Reset of the sub-unit when a related command is received from DPU. |
| **SPU-OBS-SW8** | The SPU HLSW shall support the Peak-up procedure and the interface related to this specific SW. |
| **SPU-OBS-SW9** | The SPU HLSW shall be able to support all the operating and observing modes described in RD006. |
| **SPU-OBS-SW10** | The SPU HLSW shall be able to generate simulated data for test purposes, triggered by DPU command. |
| **SPU-OBS-SW11** | The SPU HLSW shall be able to dump data from RAM whenever a DPU command is received. |
| **SPU-OBS-SW12** | The SPU HLSW shall be able to load data to RAM whenever a DPU command is received. |
| **SPU-OBS-SW13** | The SPU HLSW shall be able to check a specific RAM area whenever a DPU command is received. |
| **SPU-OBS-SW14** | The SPU HLSW shall be able to write detector selection tables and detector constant tables to RAM. |
| **SPU-OBS-SW15** | The SPU HLSW shall be able to perform the Bolometer Background Cancelling mode whenever a DPU command is received. |

## 3.2. Constraint Requirements

### 3.2.1. Communication Requirements

| ID | Requirement |
|---|---|
| **SPU-OBS-CR1** | The SPU HLSW shall provide the capability to read, individually and from the DEC/MEC header each decision, which may lead to any switching activity. |
| **SPU-OBS-CR2** | Data processing shall be faster than data acquisition and transmission. |
| **SPU-OBS-CR3** | The SPU HLSW shall be able to transmit compressed and / or uncompressed data to DPU. (Reduction only, compression only, raw data from selected detectors, compressed selected raw data or reduced and compressed data). |
| **SPU-OBS-CR4** | The transmission of compressed and / or uncompressed data to DPU should be performed via data blocks that fit into the telemetry source packet. |
| **SPU-OBS-CR5** | The compressed data packet structure should fulfil SPU-to-DPU protocol requirements. |
| **SPU-OBS-CR6** | The SPU HLSW should be able to receive raw data packets from DEC/MEC. |
| **SPU-OBS-CR7** | The SPU HLSW shall be able to cope with the hardware limitations. |
| **SPU-OBS-CR8** | The SPU HLSW shall be able to acknowledge the reception of all DPU commands. |
| **SPU-OBS-CR9** | The SPU HLSW shall be able to send HK at a regular rate compatible with the overall PACS HK rate. |
| **SPU-OBS-CR10** | Status information for link connection with DEC/MEC shall be made available to DPU in the SPU HLSW HK. |
| **SPU-OBS-CR11** | Status information for an “Are You Alive?” check by the DPU shall be made available in the SPU HLSW HK. |

### 3.2.2. Telemetry Rate Requirements

| ID | Requirement |
|---|---|
| **SPU-OBS-TM1** | The SPU HLSW shall be able to support a total output science data rate of 120 Kbits/s averaged over 24 hours. |
| **SPU-OBS-TM2** | The SPU HLSW shall be able to support a burst mode up to 300 Kbits/s for the output telemetry rate. |
| **SPU-OBS-TM3** | The SPU HLSW shall be able to support the TM rate in the PACS parallel mode by integrating over a predefined set of readouts. |
| **SPU-OBS-TM4** | The SPU HLSW shall be able to provide the nominal HK packets concerning the compression results whenever available. |
| **SPU-OBS-TM5** | The science packets shall be sent in blocks, which fit into the telemetry packet conforming to RD007. |